

ACLU1&ACLU2


(G40-70 & G50-70)

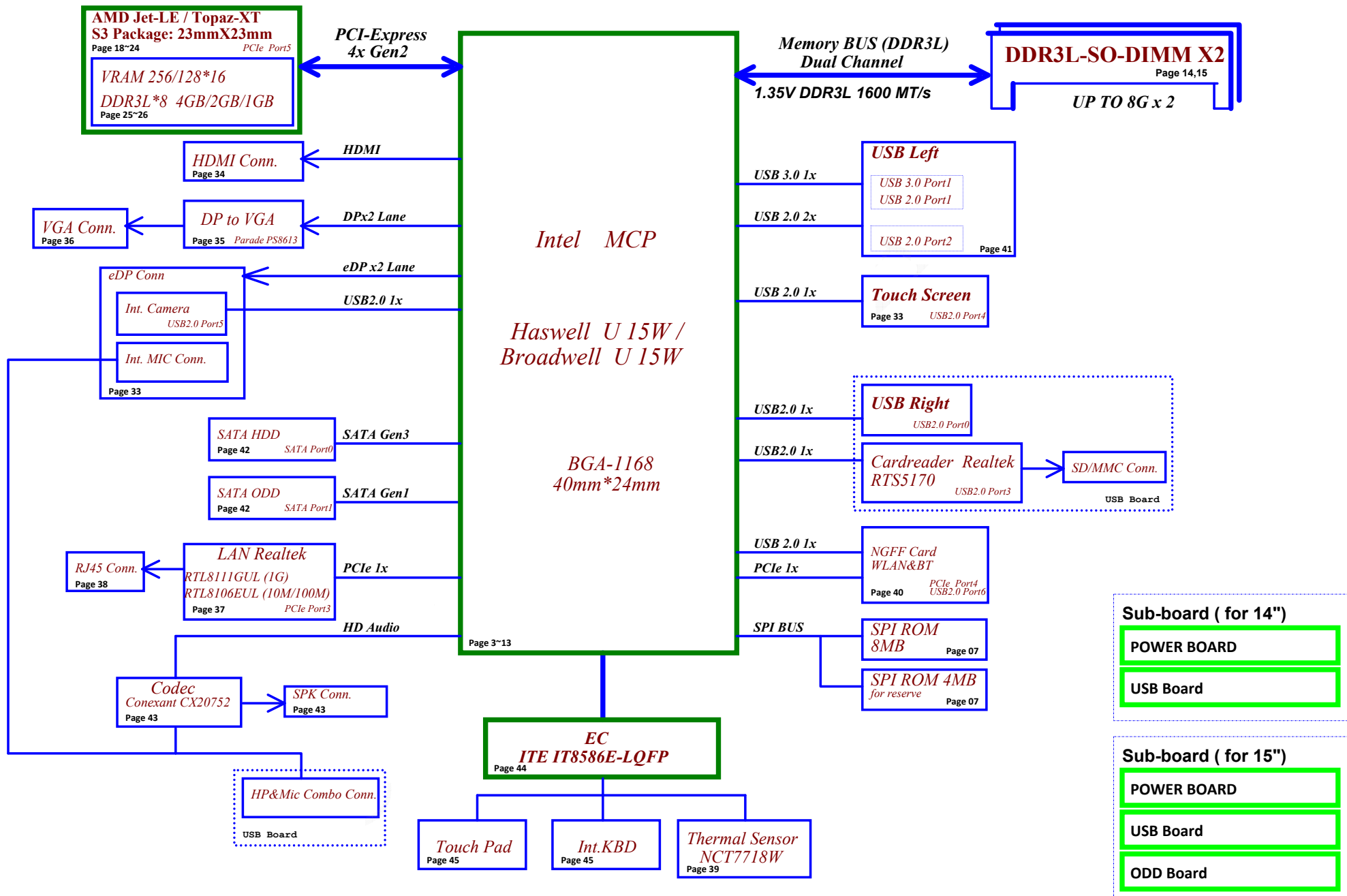
NM-A271 Rev 1.0 Schematic

Intel Haswell/Broadwell U-Processor with DDRIII L + AMD Jet-LE/Topaz-XT GPU

2013-12-17

REV:1.0

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Cover Page			
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				Date:	Thursday, December 19, 2013	Sheet	1 of 59



Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State					
	B+	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS +3VS +1.5VS +1.35VS +1.05VS +0.675VS CPU_CORE +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0 EHCI1		USB 3.0 XHCI	
0	USB Port (Right Side)		
1	USB Port1 (Left Side)	1	USB Port1 (Left Side)
2	USB Port2 (Left Side)	2	
3	Cardreader	3	
4	TOUCH PANEL	4	
5	Camera		
6	NGFF(WLAN)		
7			

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
100M@	100M LAN Part
14@	For 14" part
15@	For 15" part
AOAC@	AOAC support part
GIGA@	GIGA LAN Part
JET@	For AMD Jet GPU part
ME@	ME part(connector, hole)
PX@	Discrete GPU SKU part
RANKA@	For VRAM RankA part
RANKB@	For VRAM RankB part
TOPAZ@	For AMD Topaz GPU part
TS@	For support touch panel sku part
UMA@	UMA SKU part
H2@	Hynix 128Mx16 VRAM part
H4@	Hynix 256Mx16 VRAM part
M2@	Micron 128Mx16 VRAM part
M4@	Micron 256Mx16 VRAM part
S2@	Samsung 128Mx16 VRAM part
S4@	Samsung 256Mx16 VRAM part
H2GX8@	Hynix 128Mx16 VRAM x8pcs sku
H4GX4@	Hynix 256Mx16 VRAM x4pcs sku
M4GX4@	Micron 256Mx16 VRAM x4pcs sku
CD@	Cost down part

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

PCIE PORT LIST

Port	Device
1	
2	
3	LAN
4	WLAN
5	Discrete GPU
6	

EC SM Bus1 address

EC SM Bus2 address

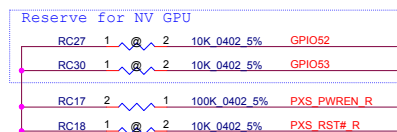
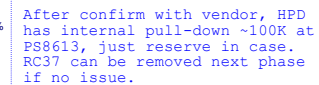
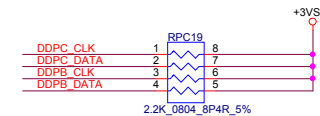
PCH SM Bus address

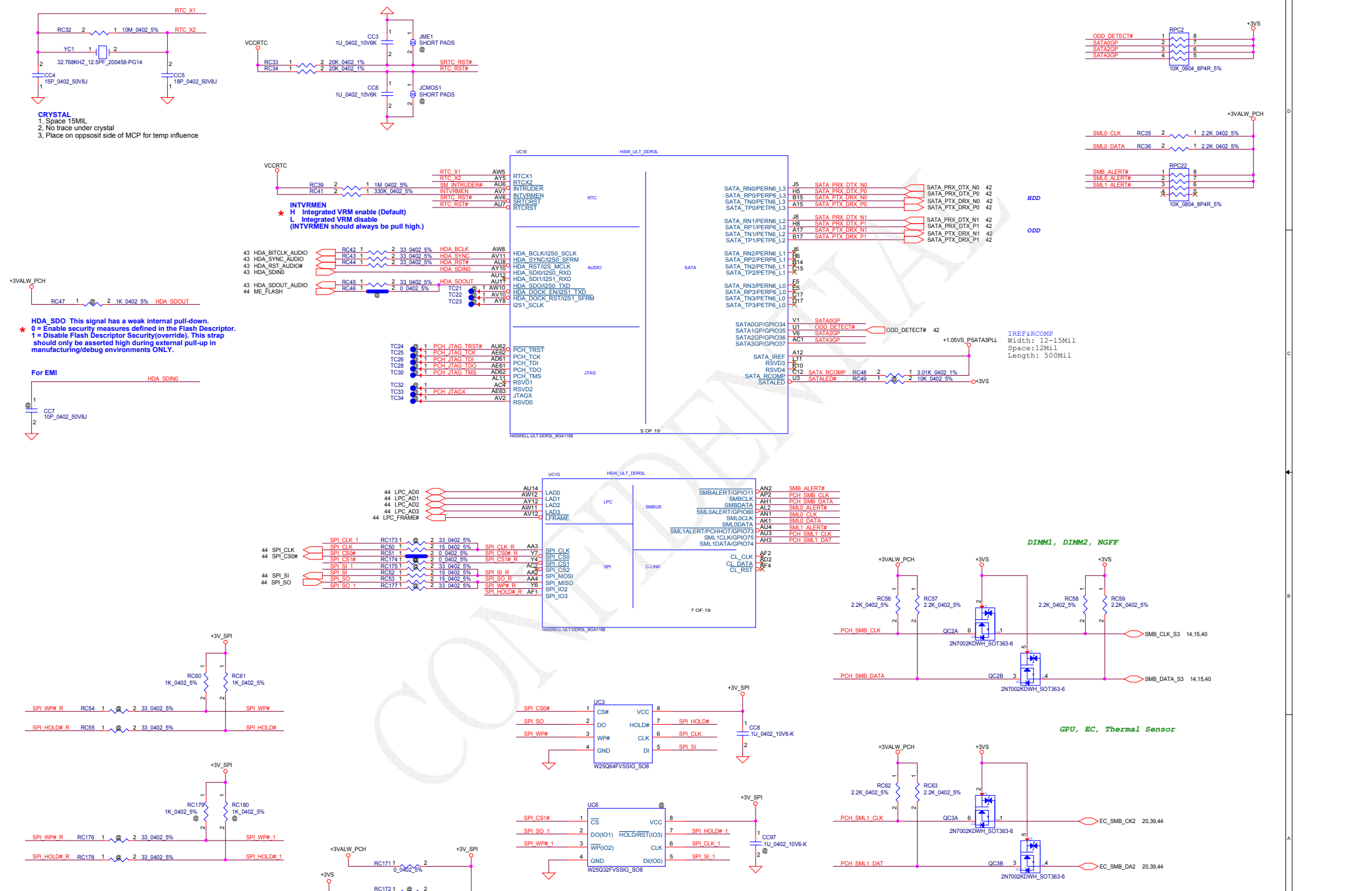
Device	Address	Device	Address
Smart Battery	0X16	Thermal Sensor NCT7718W	1001_100xb
Charger	0001 0010 b	VGA	0x41(default)
		PCH	need to update

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

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Title	Notes List
Document Number	ACL01 & ACL02
Date	Thursday, December 19, 2013
Sheet	3 of 59

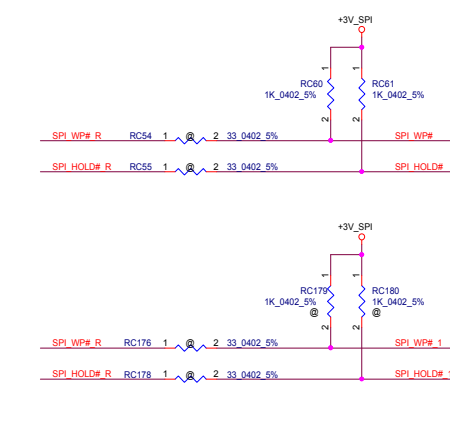




CRYSTAL
1. Space 15mil
2. No trace under crystal
3. Place on opposite side of MCP for temp influence

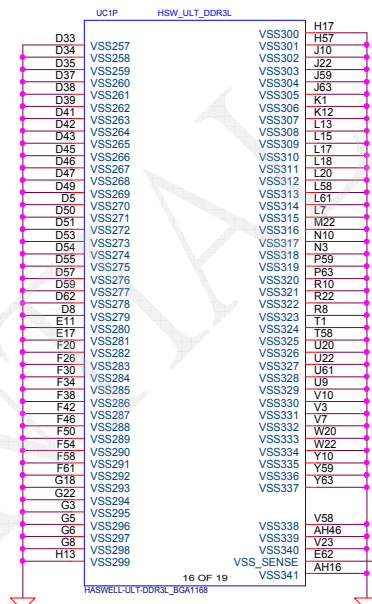
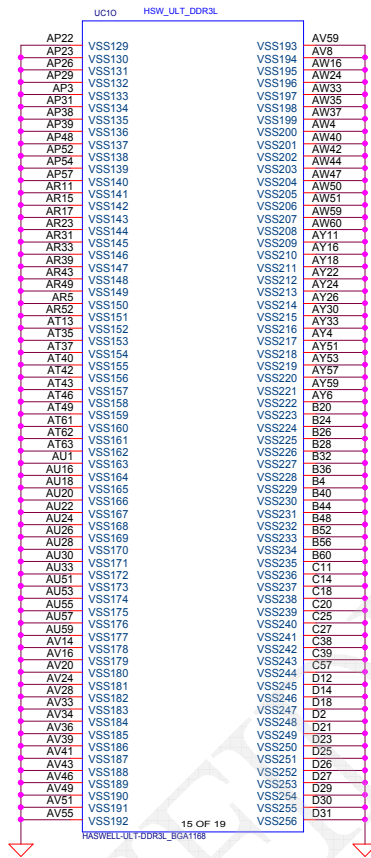
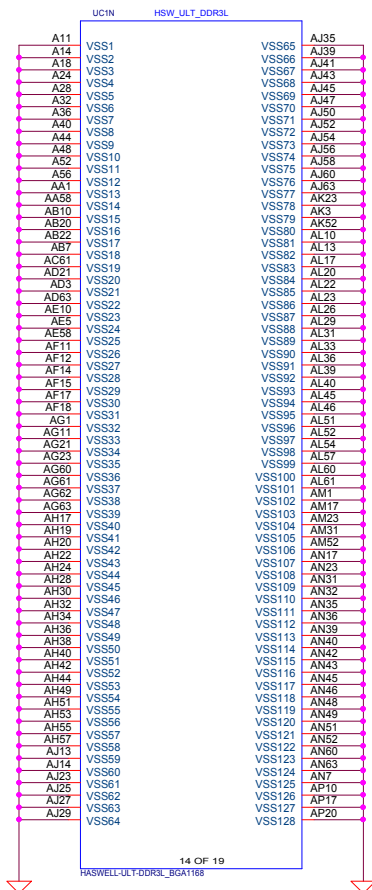
HDA_SDO This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.

For EMI
CC7
10P_0402_50V8J



+3V_SPI
1. If support DS3, connect to +3VS and don't support EC mirror code;
2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.


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C	ACL01&ACL02				1.0
Date: Thursday, December 19, 2013 Sheet 7 of 59					



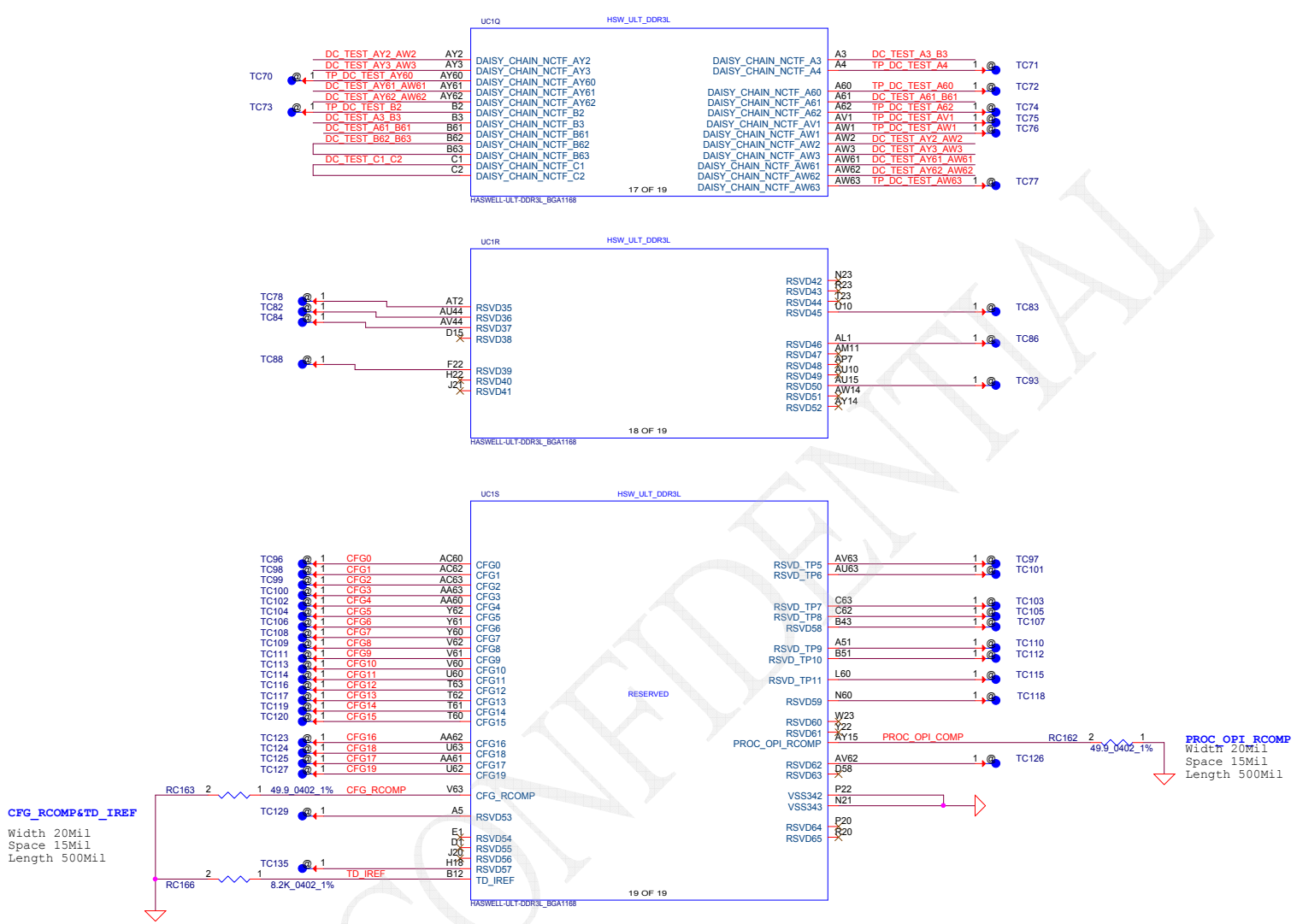
RC158 1 2 0 0402_5% CPU_VSS_SENSE 59

RC159 100_0402_1%

VSS SENSE
 Length Match: No More Than 25Mil
 Space: More Than 25Mil
 GND Reference

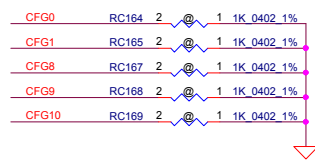
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				Date: Thursday, December 19, 2013	Sheet 12 of 59
				Rev 1.0	





CFG3
*1: Disable
0: Enable, Set DFX Enabled BIT
In Debug Interface MSR

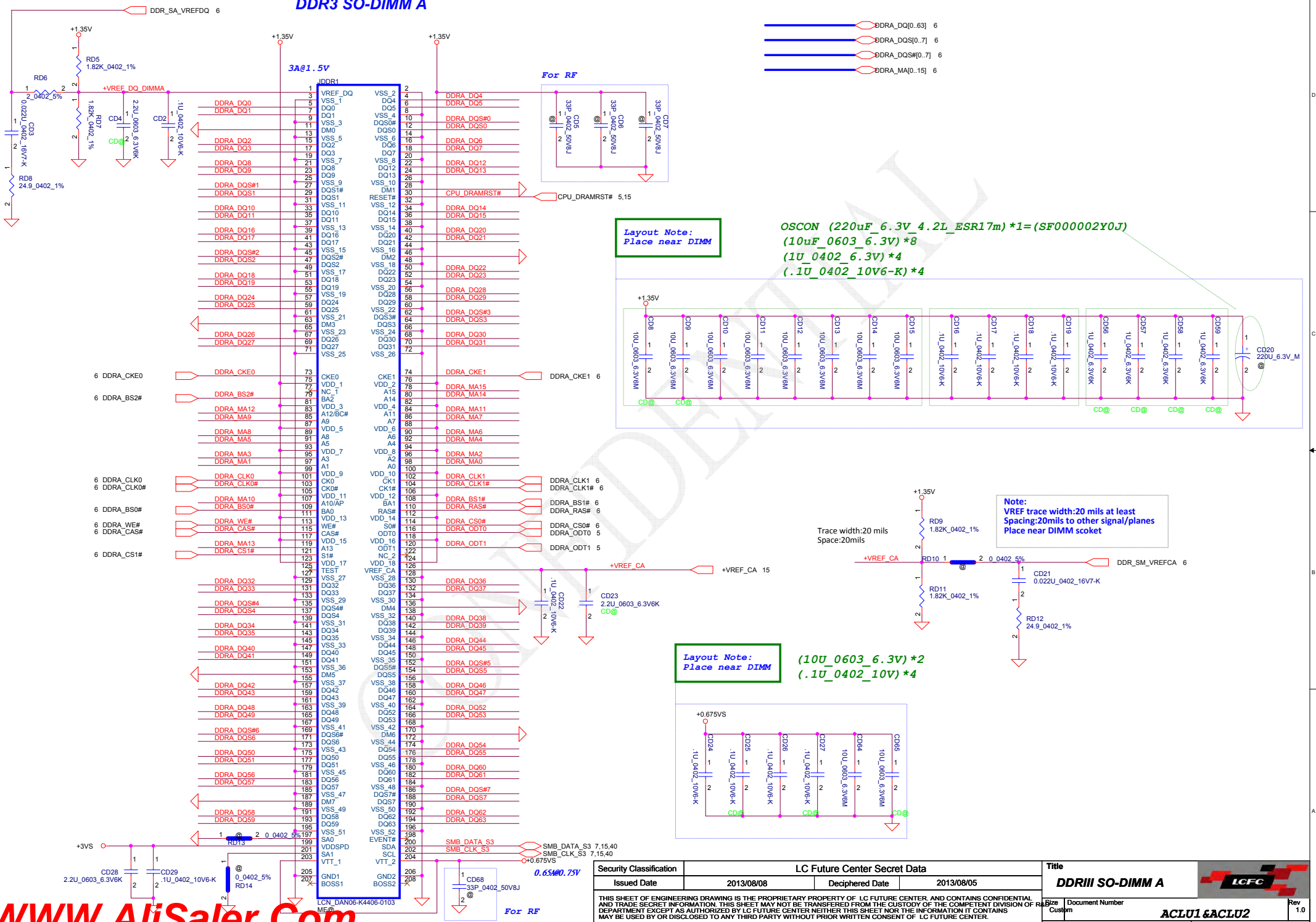
CFG4
*L: eDP enable
H: eDP disable




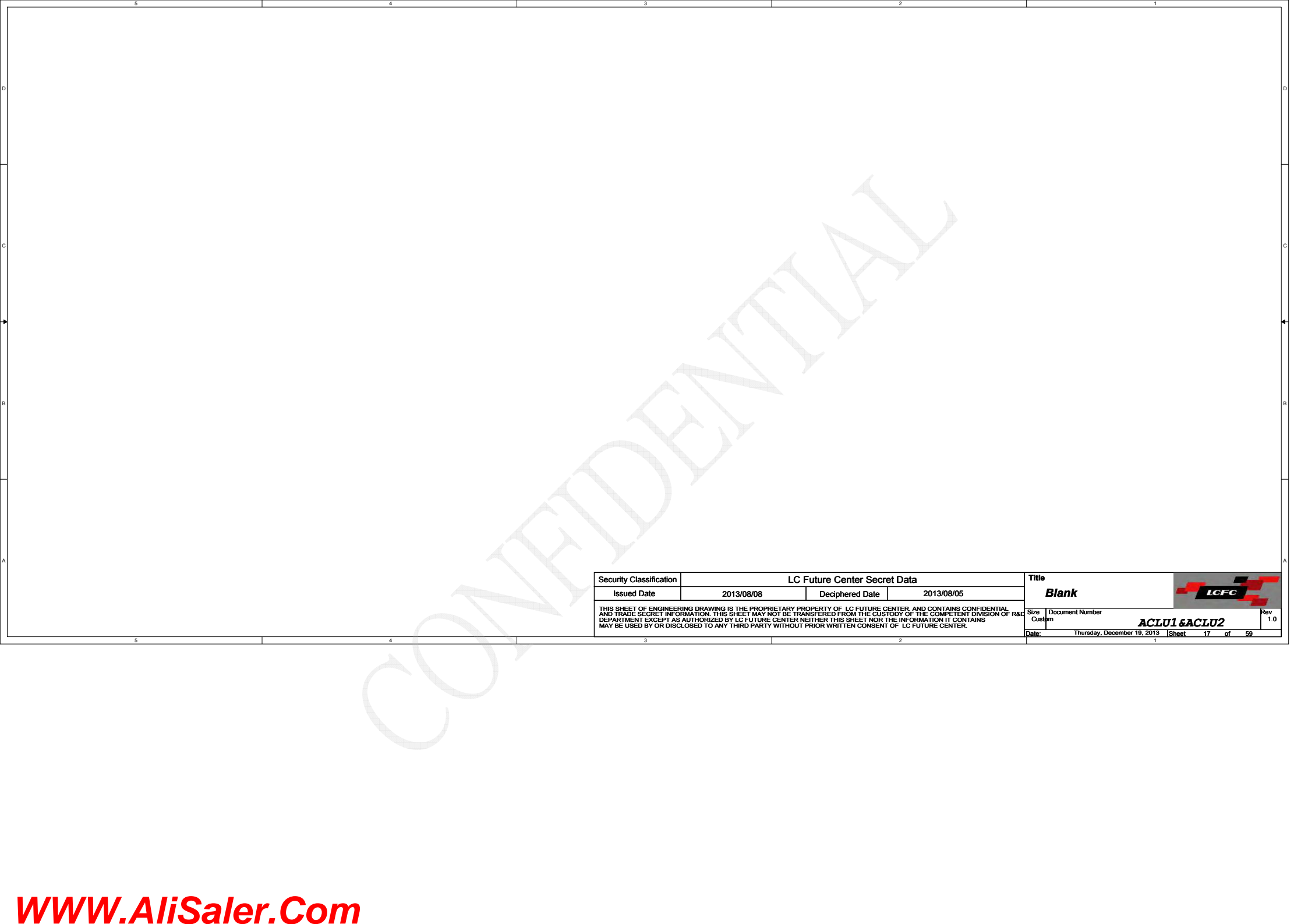
CFG_RCOMP&TD_IREF
Width 20Mil
Space 15Mil
Length 500Mil


PROC_OPI_RCOMP
Width 20Mil
Space 15Mil
Length 500Mil

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DDR3 SO-DIMM A

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				Date:	Thursday, December 19, 2013	Rev 1.0
3		1		2		Sheet 16 of 59

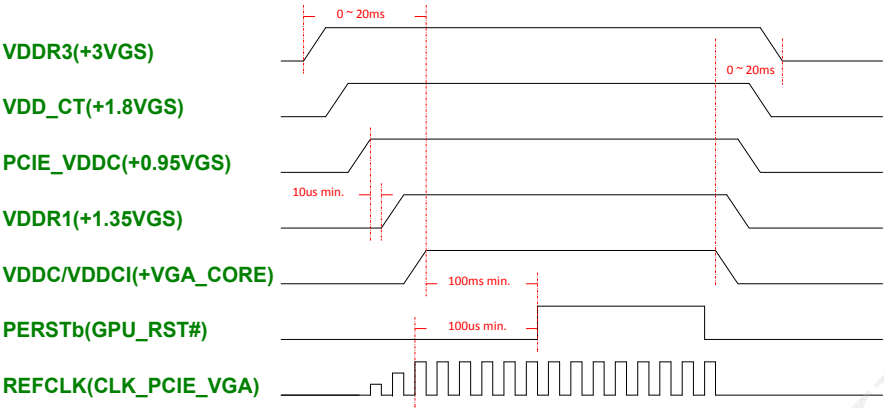


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Custom				ACLU1 & ACLU2		
Date:		Thursday, December 19, 2013		Sheet		17 of 59
				1		

Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs. It is recommended that the 3.3-V rail ramp up first. The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μs before VDDC, VDDCI, and VMEMIO start to ramp up. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μs). For power down, reversing the ramp-up sequence is recommended.



CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE			
MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 100 = 256MB	X
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 0= Not support	X
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQ power management capability is disabled 1 = The CLKREQ power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	X
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	X
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 000 = Hynix 256M*16 001 = Hynix 128M*16 100 = Samsung 256M*16 011 = Samsung 128M*16 010 = Micron 256M*16 111 = Micron 128M*16	X
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable. 111= No usable endpoints.	11

VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV33	PD resistor RV36
128Mx16	Hynix H5TC2G63FFR-11C	100	4.53K	4.99K
	Micron MT41J128M16JT-093G	111	4.75K	NC
	Samsung K4W2G1646Q-BC1A	110	3.4K	10K
256Mx16	Hynix H5TC4G63AFR-11C	000	NC	4.75K
	Micron MT41J256M16HA-093G	010	4.53K	2K
	Samsung K4W4G1646D-BC1A	001	8.45K	2K
	Micron MT41K256M16HA-107G	011	6.98K	4.99K

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VGA Notes List

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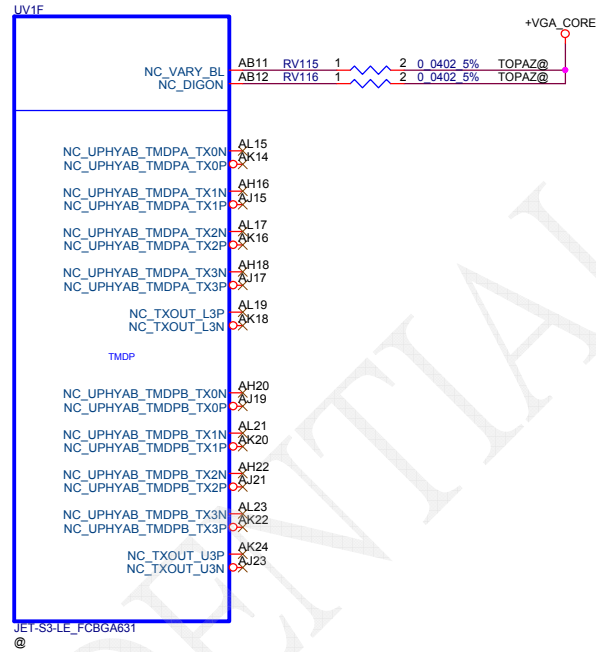
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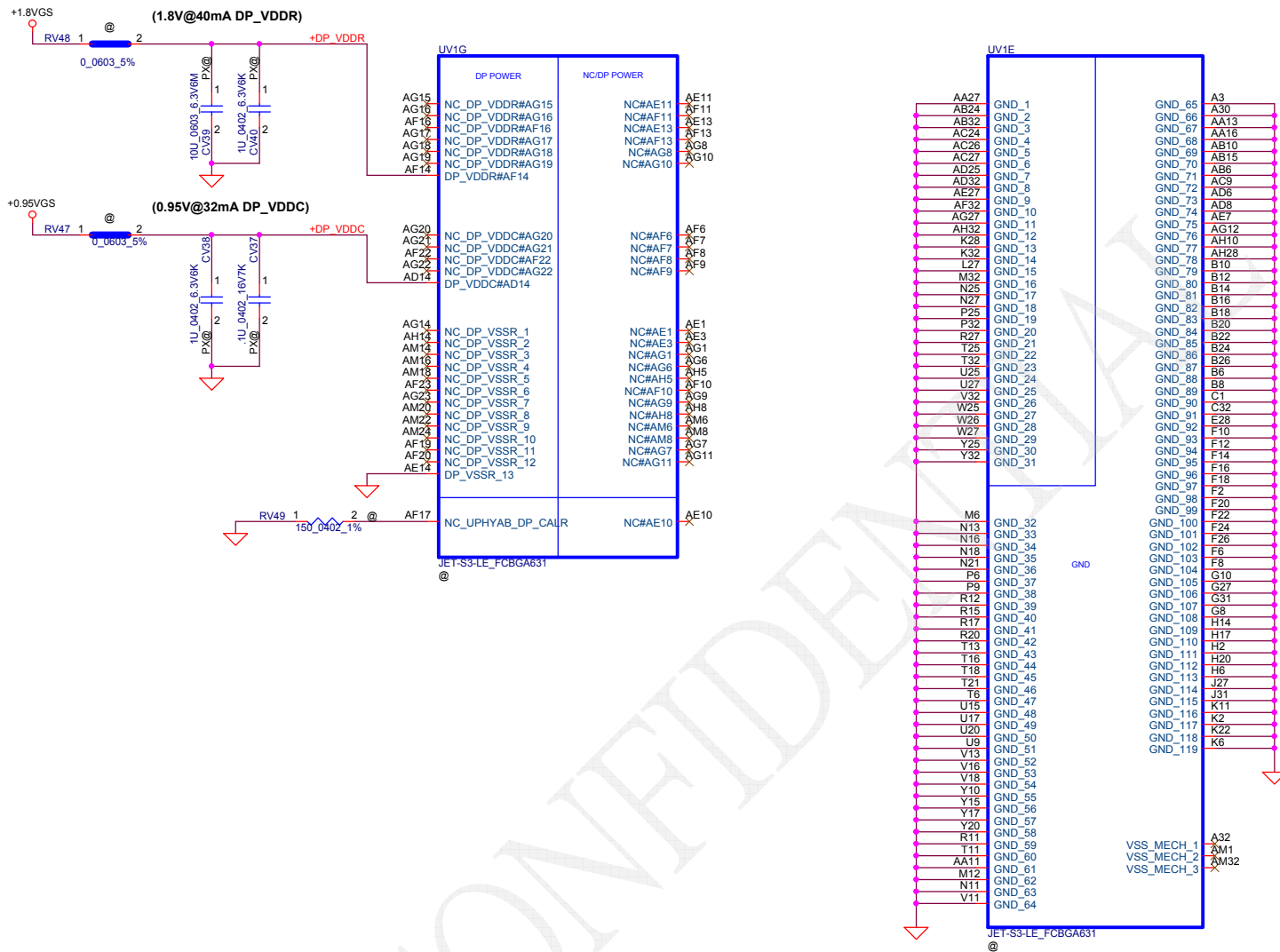
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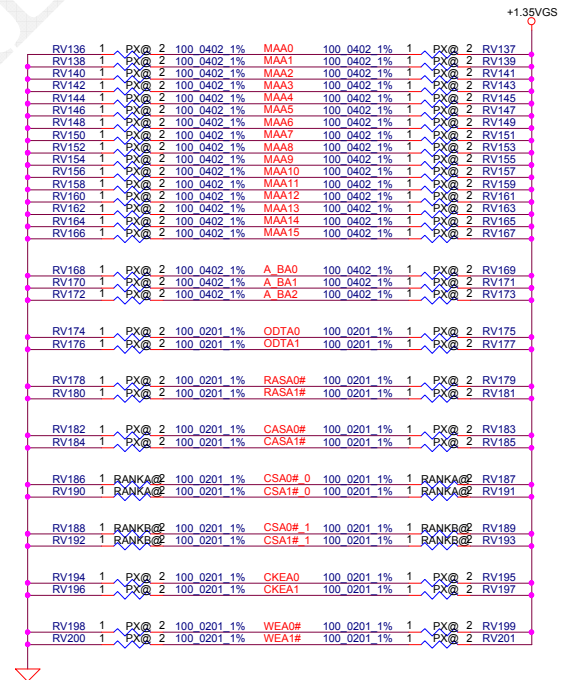
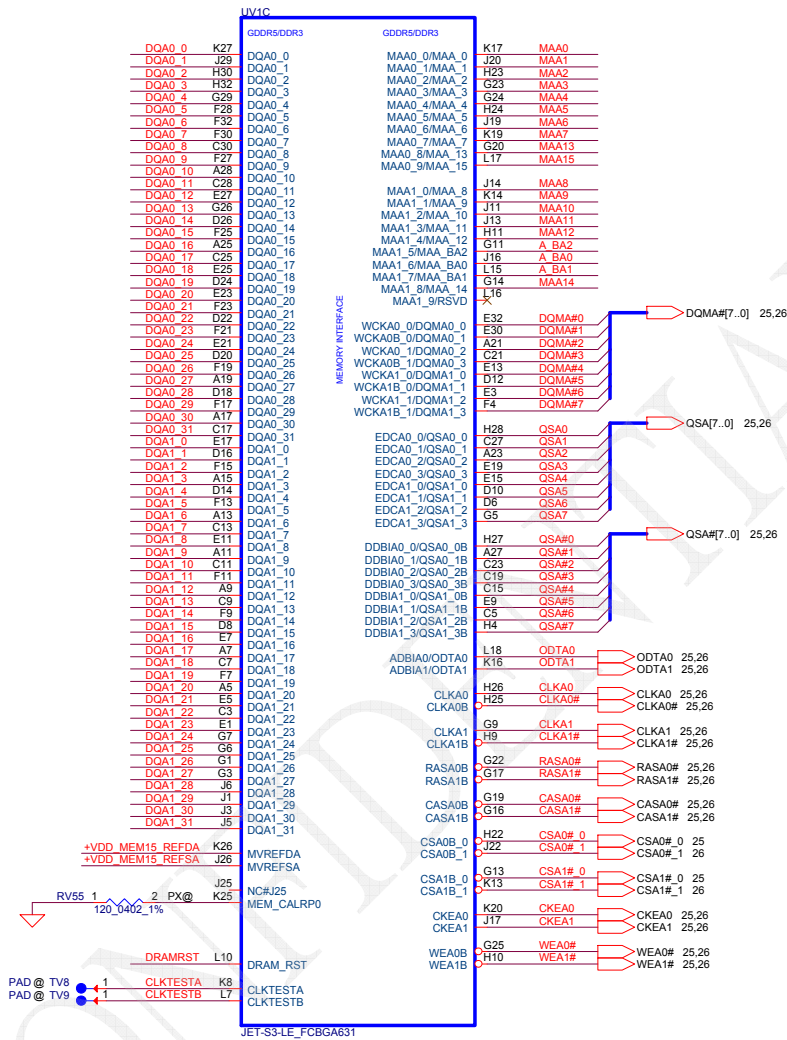
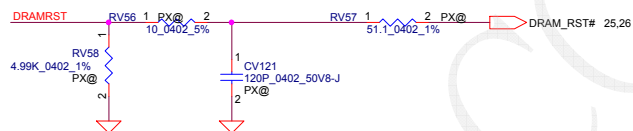
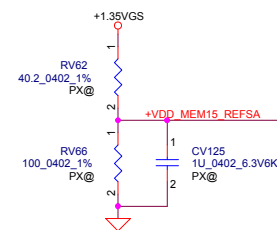
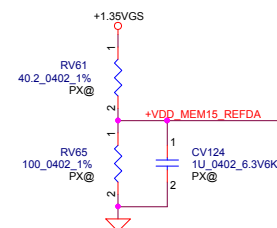
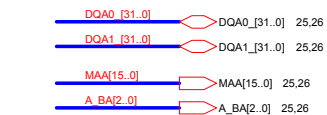



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				Sheet 21	of 59

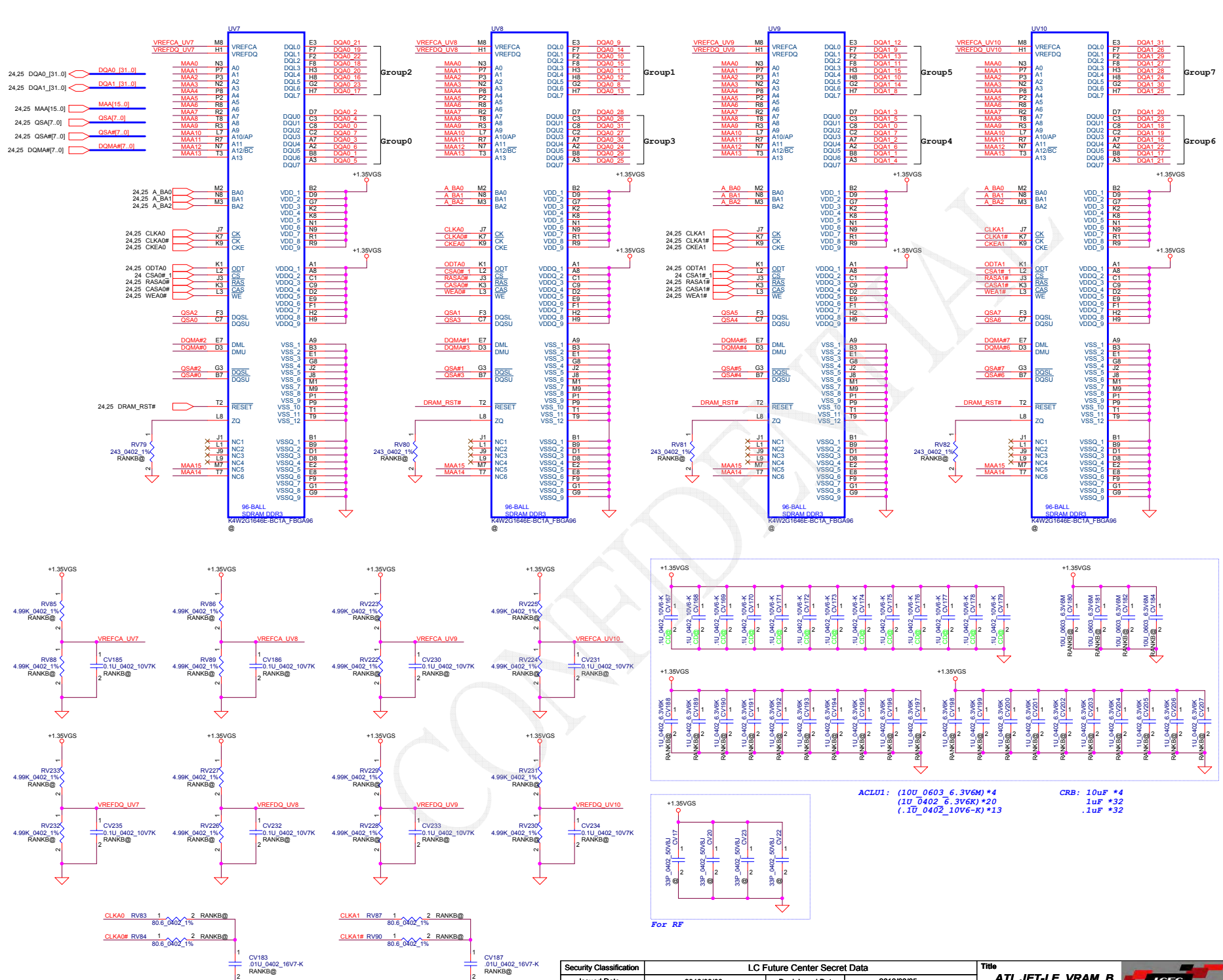


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				Date: Thursday, December 19, 2013	Sheet 22 of 59





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Date:		Thursday, December 19, 2013		Sheet		24		of 59	

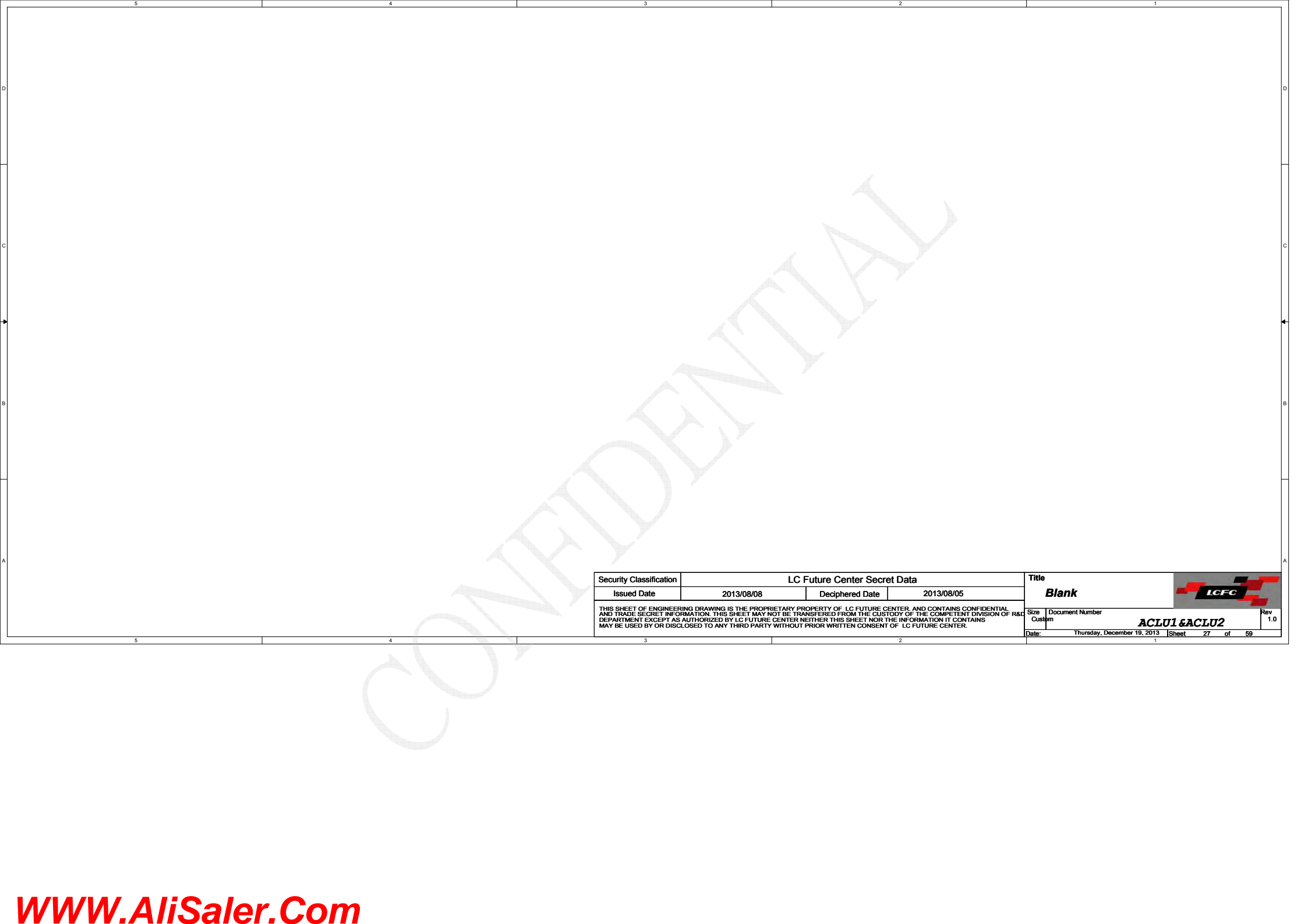



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				Date Thursday, December 15, 2013	
				Sheet 26 of 59	


ACLUI: (10U_0603_6_3V6M)*4
(1U_0402_6_3V6K)*20
(1U_0402_10V6-K)*13

CRB: 10uF *4
1uF *32
1uF *32

For RF





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				Document Number ACLU1 & ACLU2	Rev 1.0
				Date: Thursday, December 19, 2013	Sheet 27 of 59

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Date:										Thursday, December 19, 2013		Sheet 28 of 59			

5	4	3	2	1
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B				B
A				A
5	4	3	2	1

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Date:										Thursday, December 19, 2013		Sheet		30 of 59	

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Date

Thursday, December 19, 2013

Sheet

31

of

59

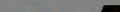
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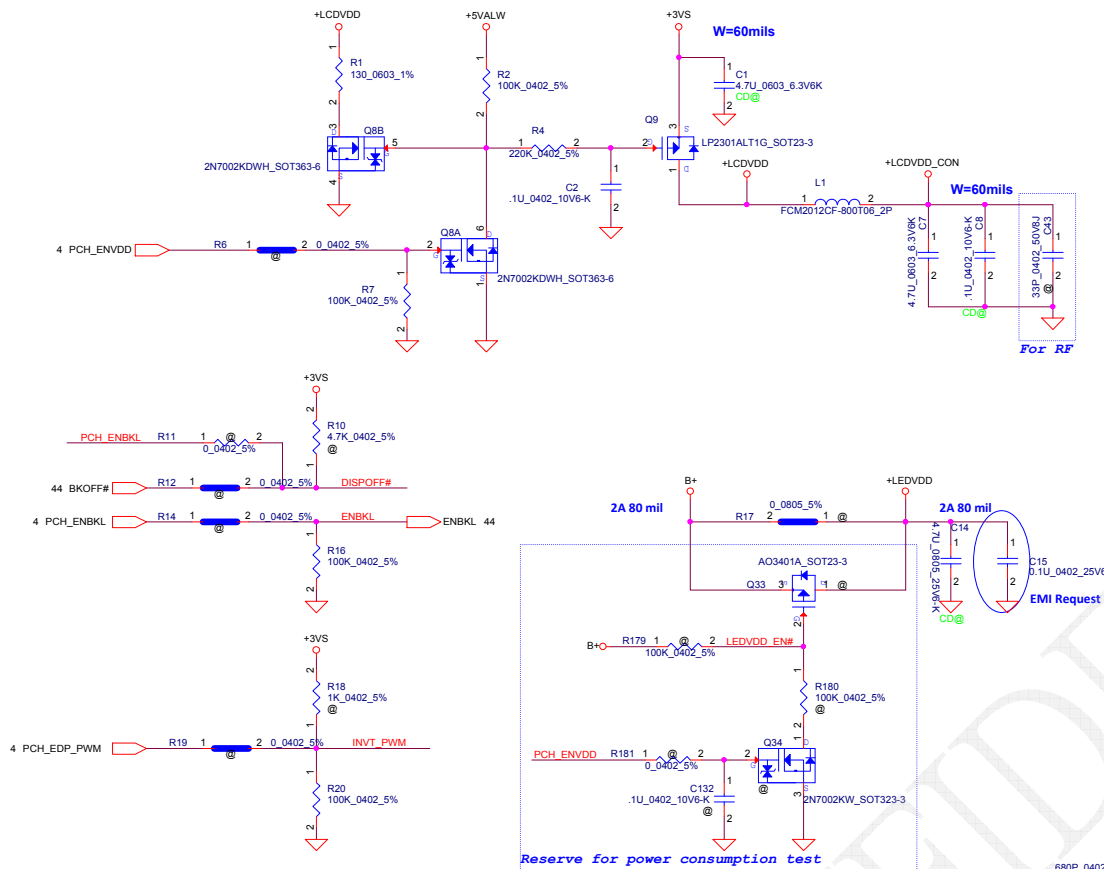
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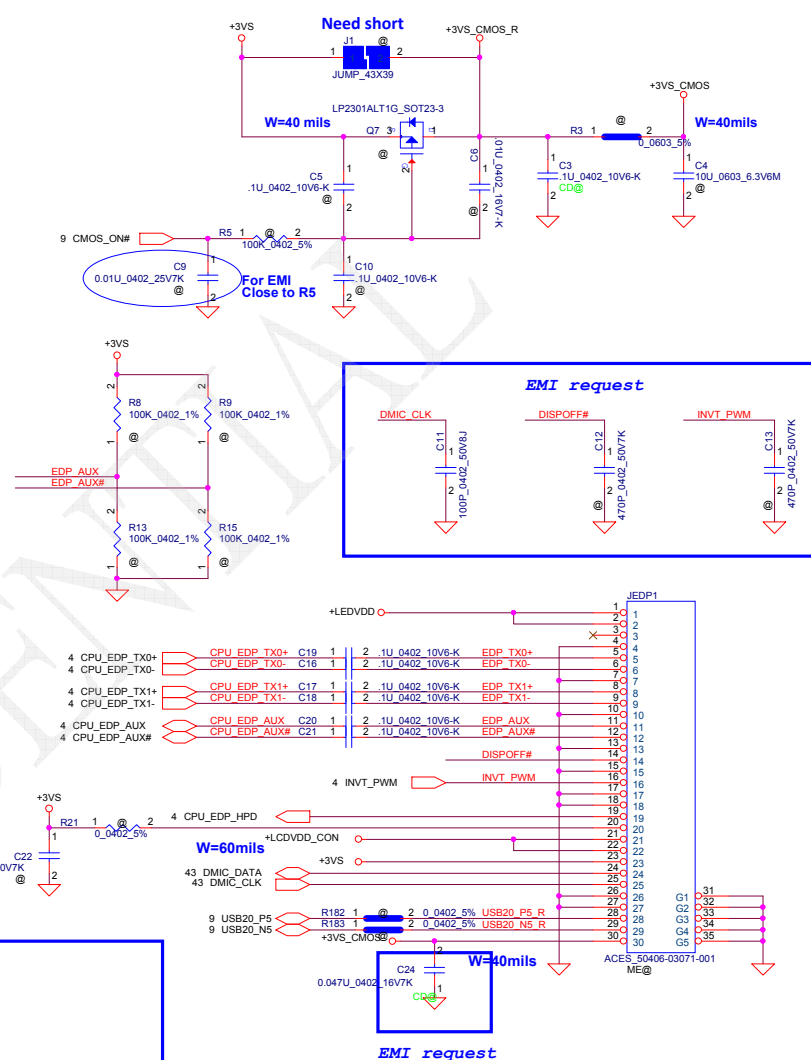
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				Date:	Thursday, December 19, 2013	<p>Rev</p> <p>1.0</p>
3		1		2		<p>Sheet</p> <p>32 of 59</p>

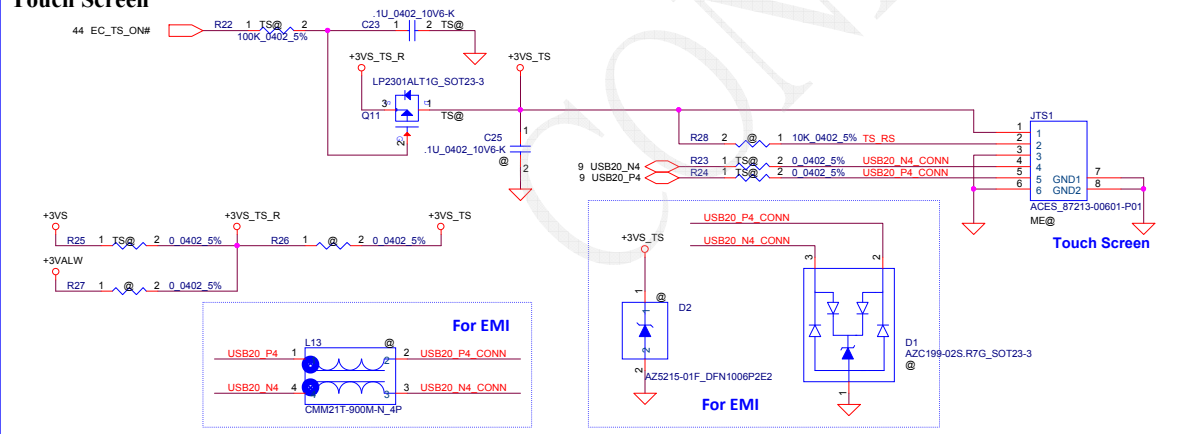
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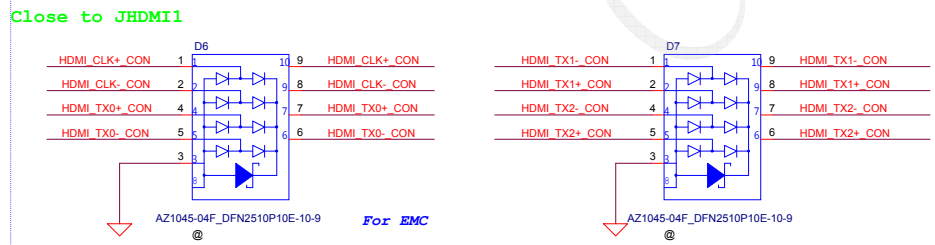
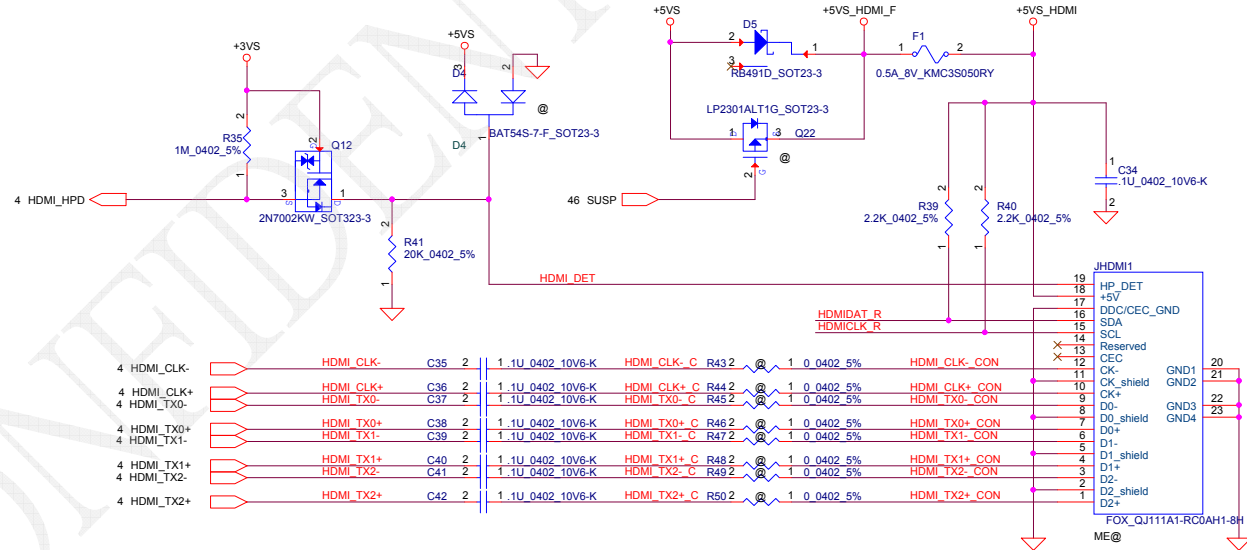
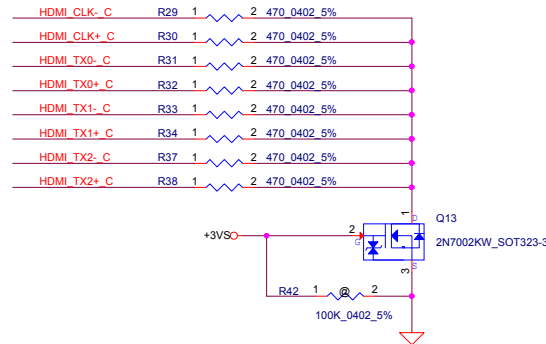
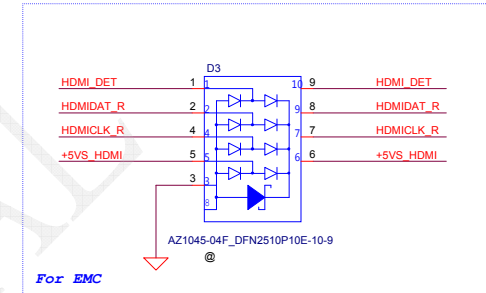
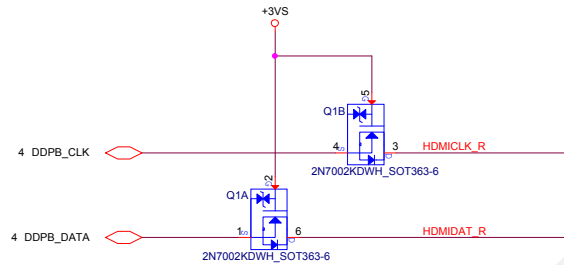
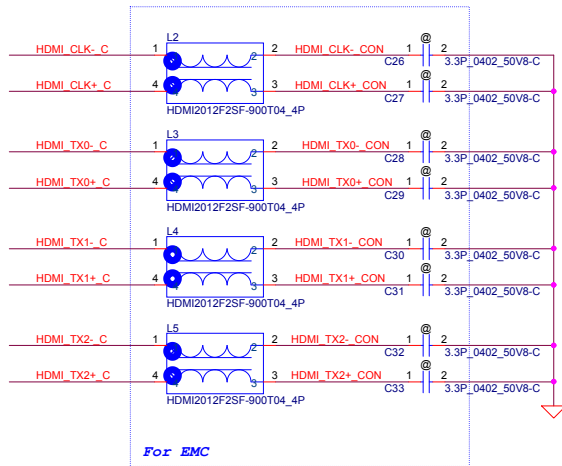
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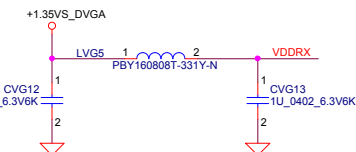
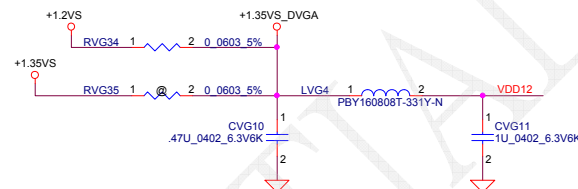
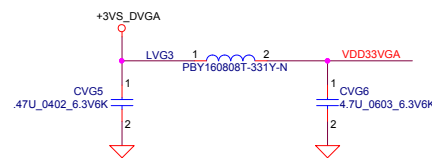
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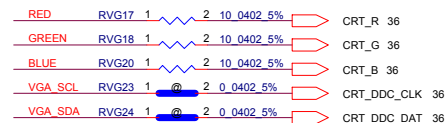
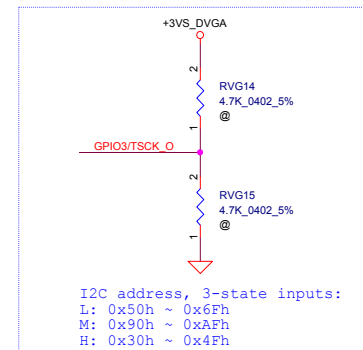
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Issued Date		Deciphered Date		eDP/ CMOS/Touch screen	
2013/08/08		2013/08/05		Rev 1.0	
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Date:		Friday, December 20, 2013		Sheet 33 of 59	



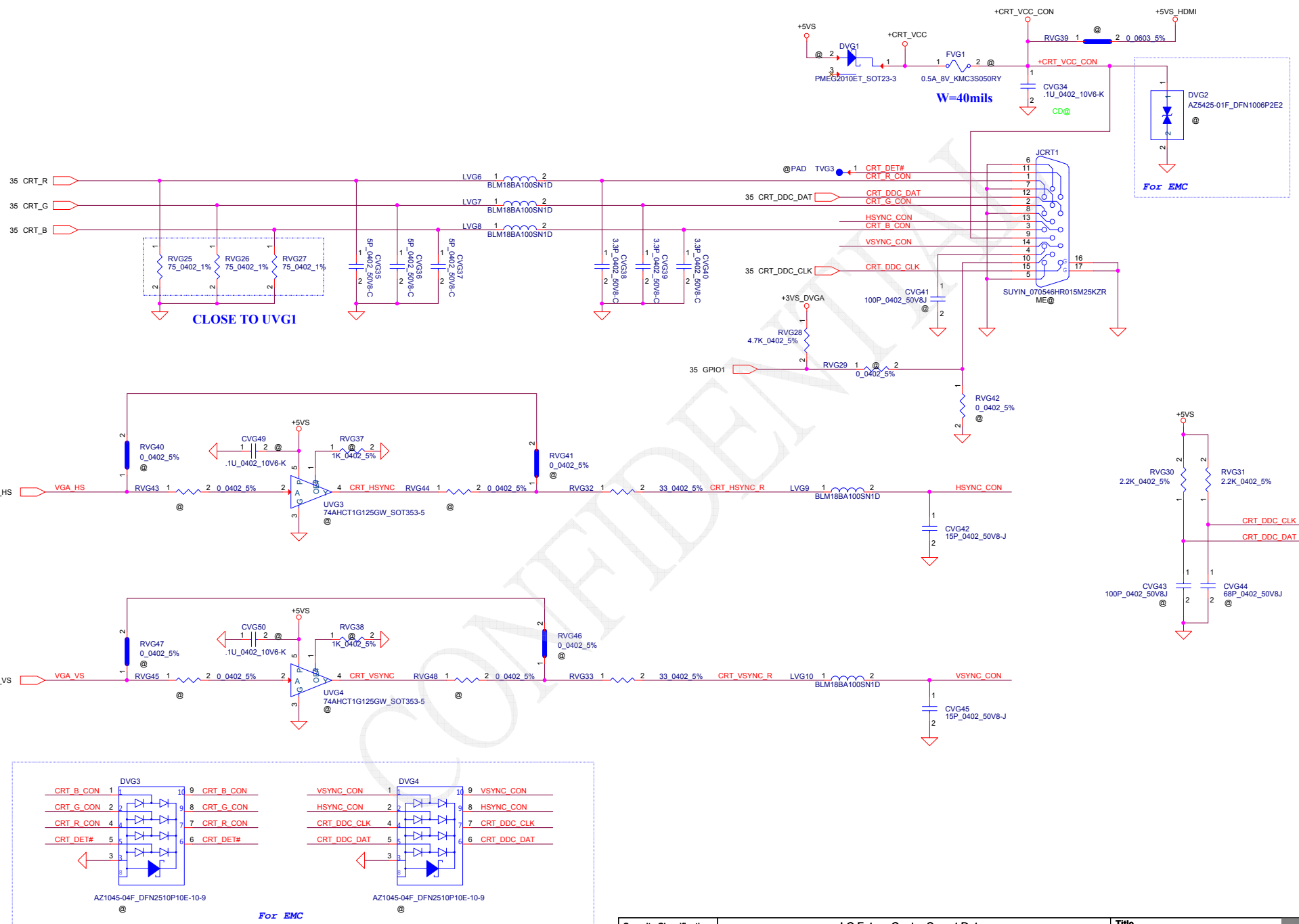
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Date: Tuesday, December 24, 2013				Sheet	34 of 59


[illegible]

.1U_0402 16V7-K
 CVG28
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 2
 .1U_0402 10V6-K
 CVG29
 CD6

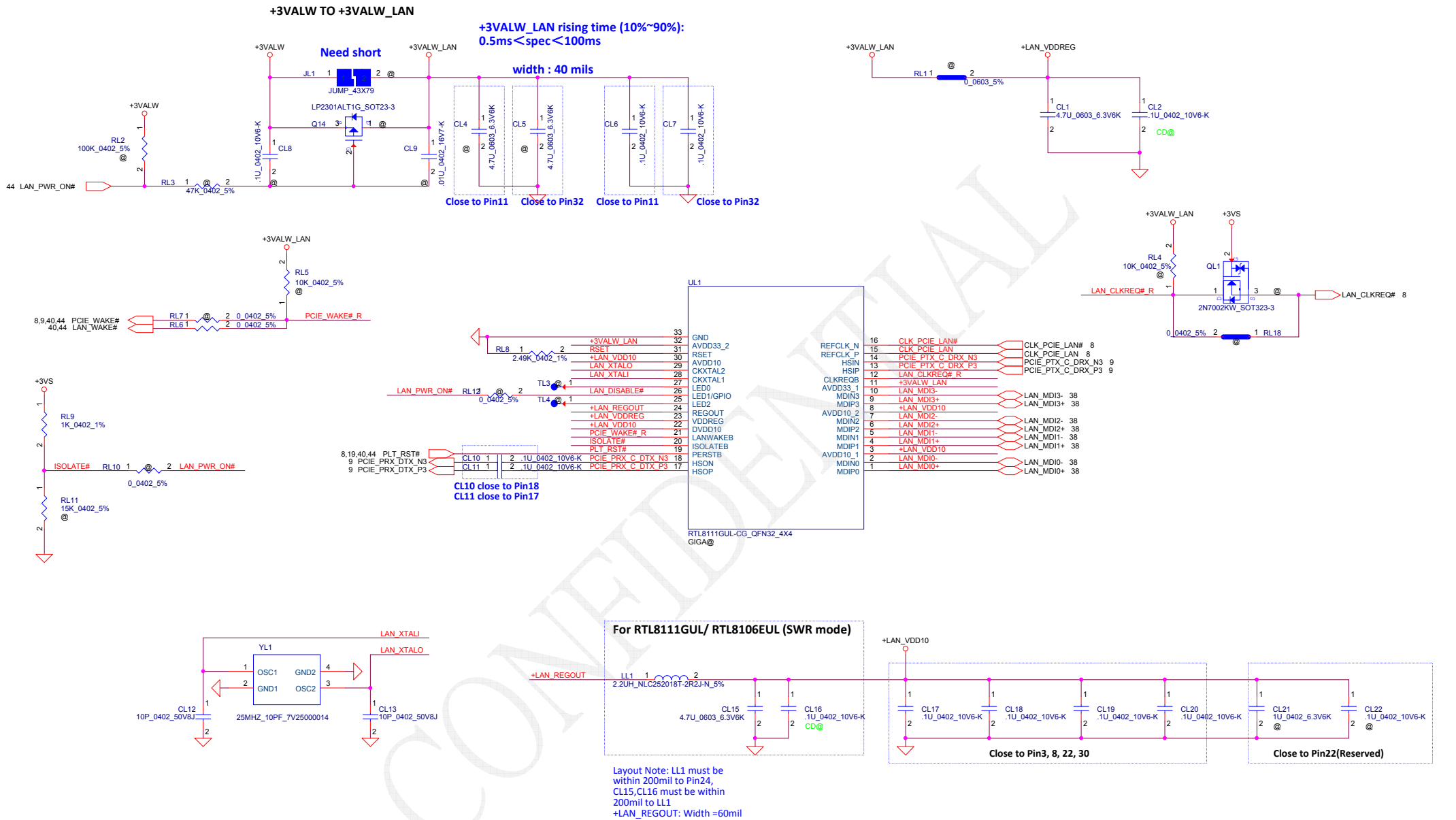


CRT Connector



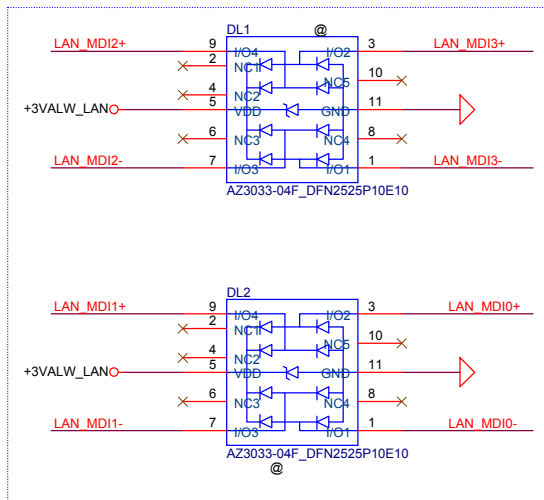
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						Custom	ACL01 & ACL02	1.0			
						Date:	Thursday, December 19, 2013	Sheet	36	of	59



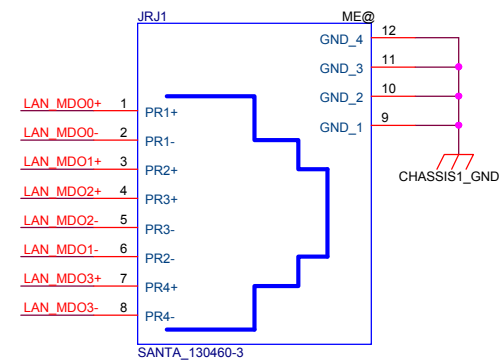
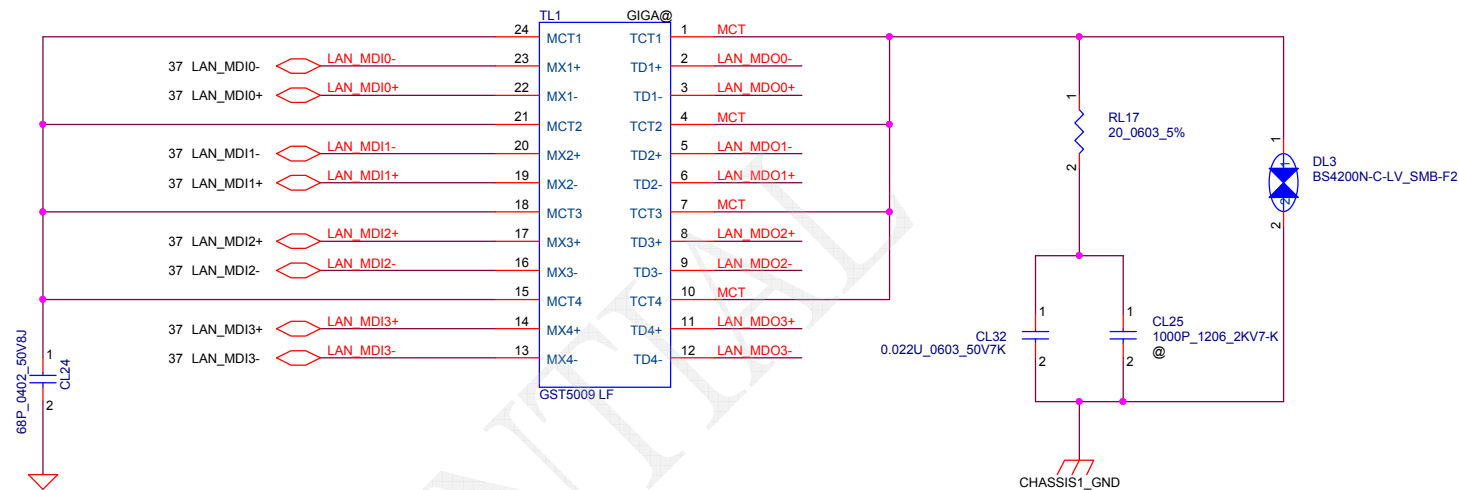
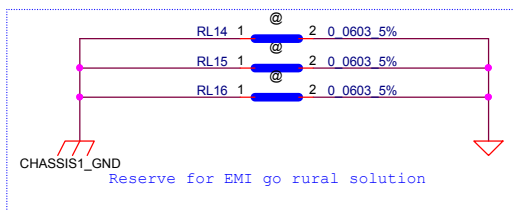



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Date:		Thursday, December 19, 2013		Sheet 37 of 59	

DL1/DL2
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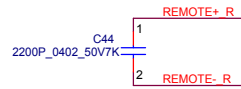


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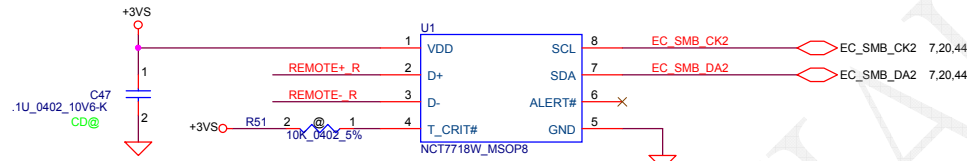


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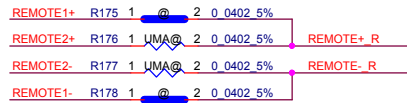
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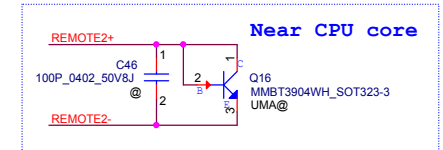
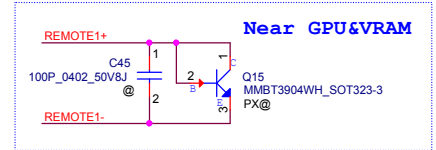
SMSC thermal sensor placed near DIMM



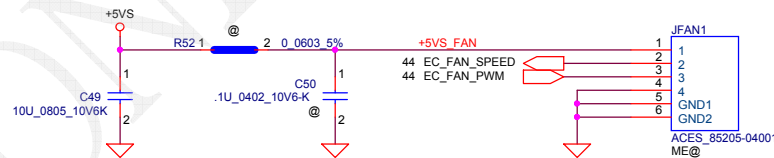
Address 1001_100xb



REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



FAN Conn




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				Date: Thursday, December 19, 2013	Sheet 39 of 59



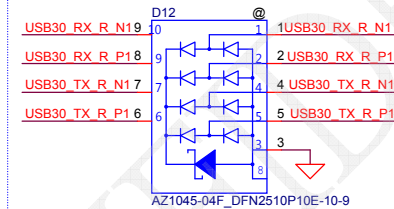
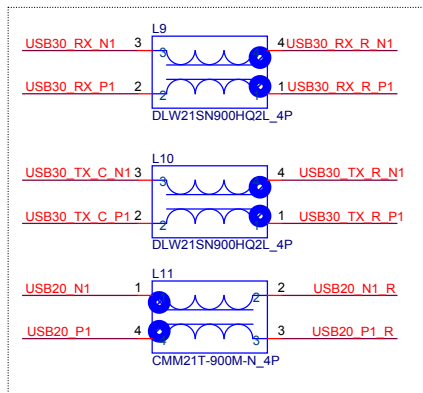
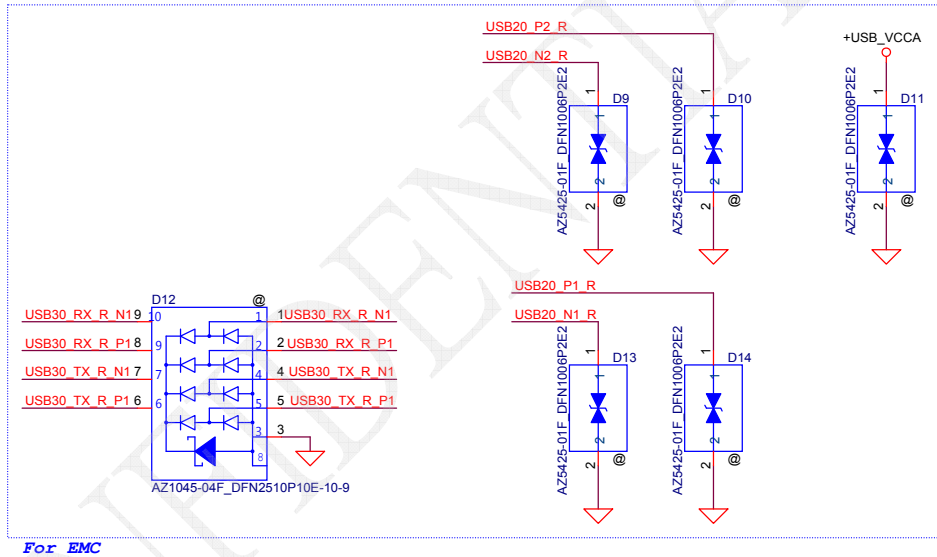
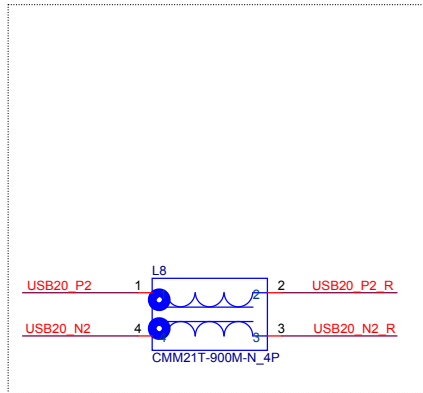
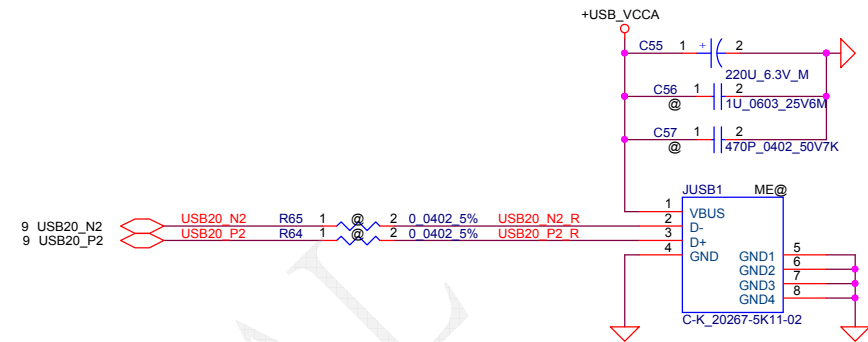
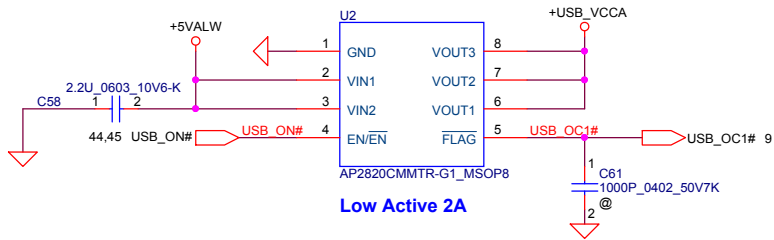
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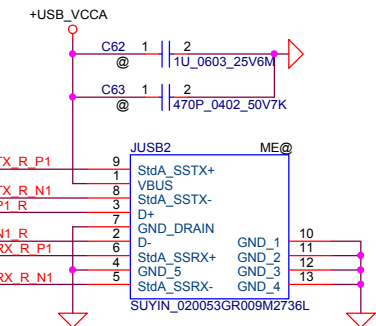
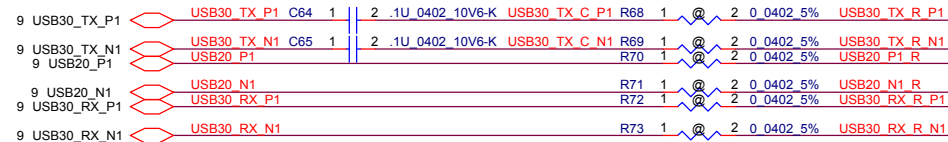


Title			
NGFF WLAN			
Size Custom	Document Number	ACLU1 & ACLU2	Rev 1.
Date:	Thursday, December 19, 2013	Sheet	40 of 59

LEFT SIDE USB3.0 PORT X2



For EMC

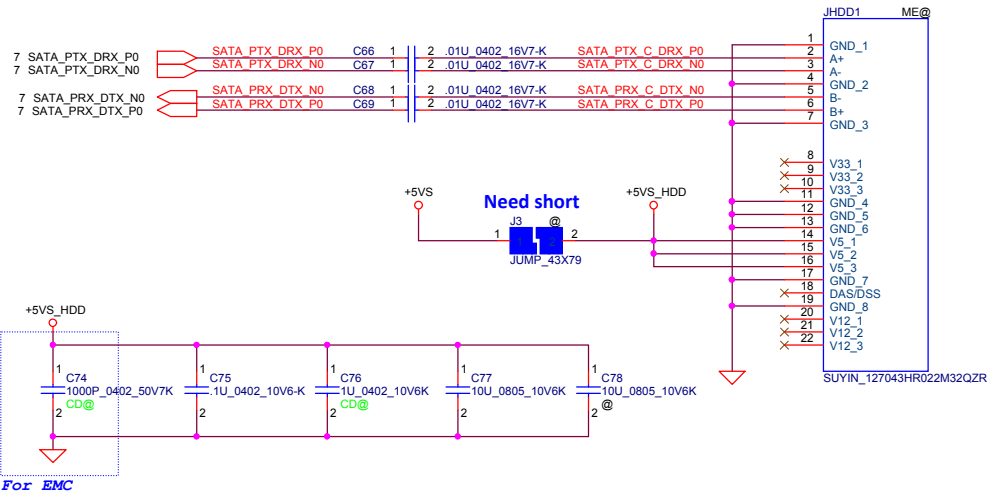


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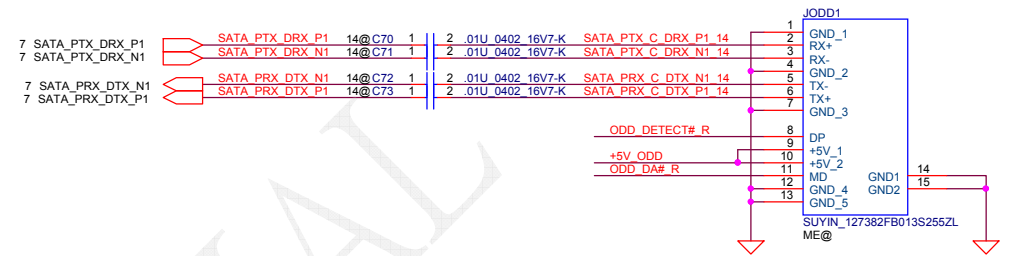
Size	Document Number	Rev
Custom	ACLU1 & ACLU2	1.0
Date:	Thursday, December 19, 2013	Sheet 41 of 59



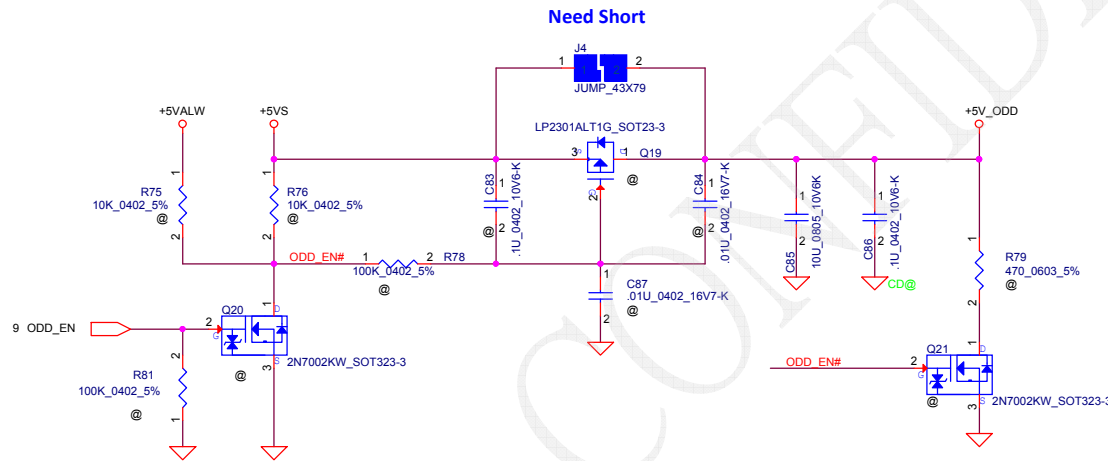
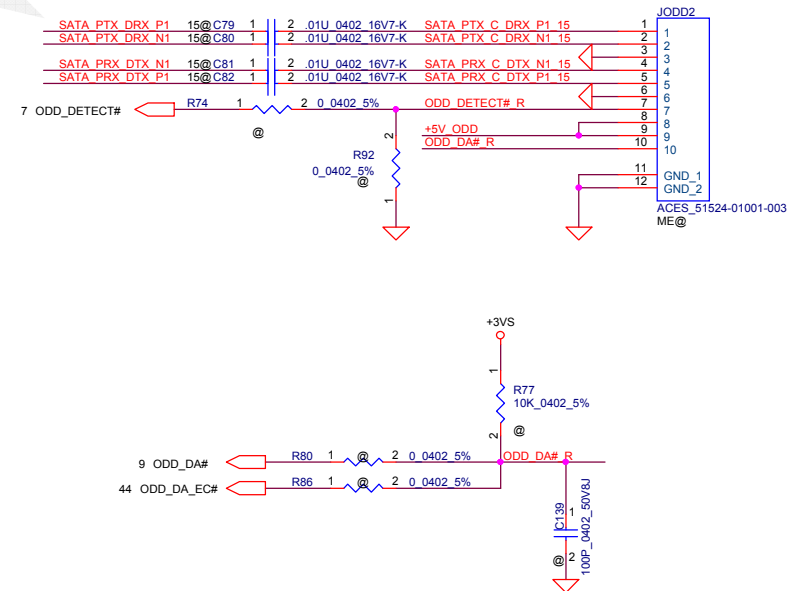
SATA HDD Conn.



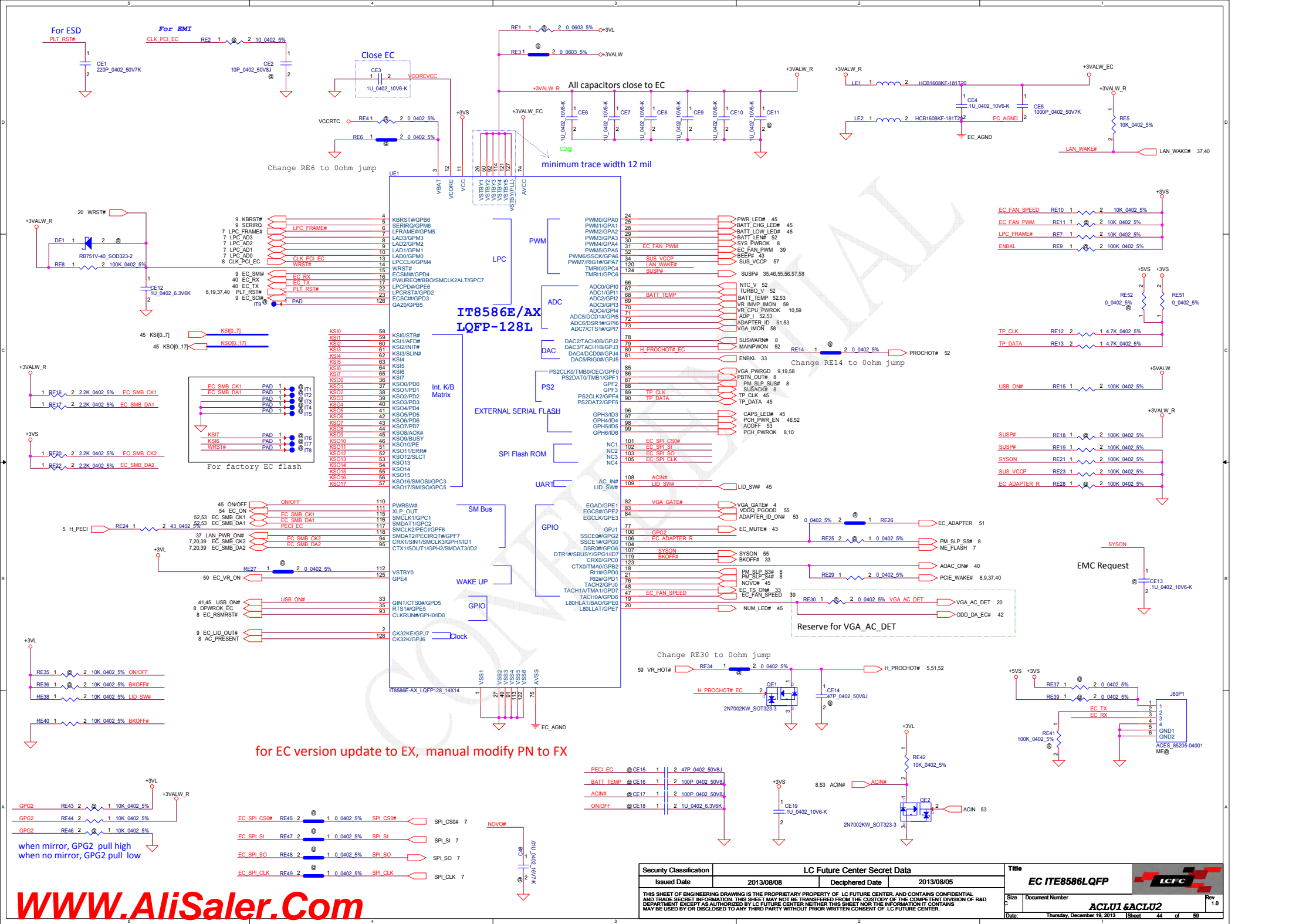
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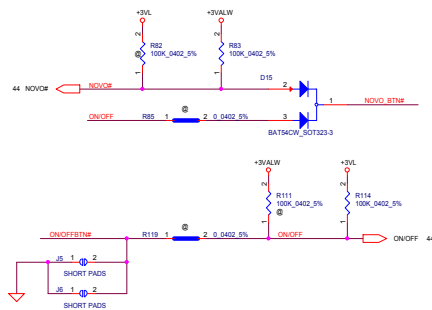
FOR 15" SATA ODD FFC Conn



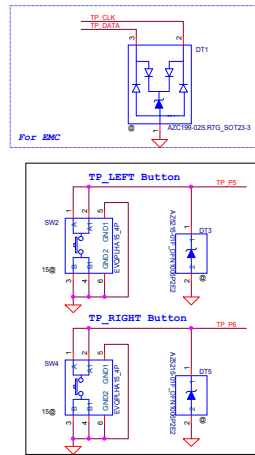
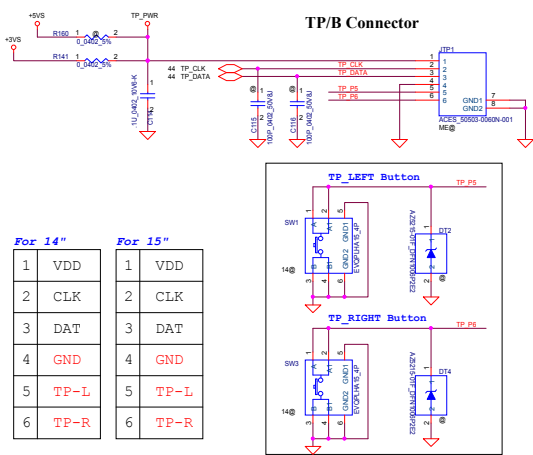
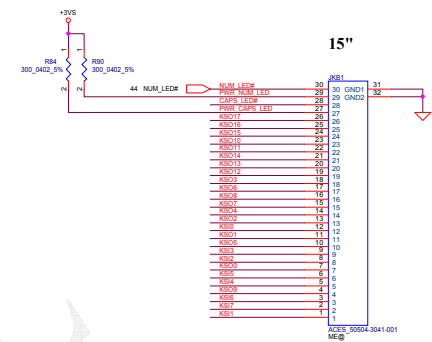
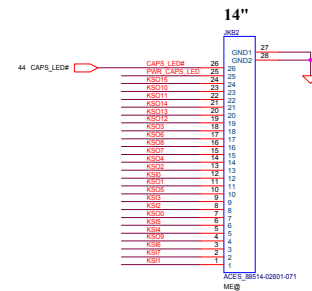
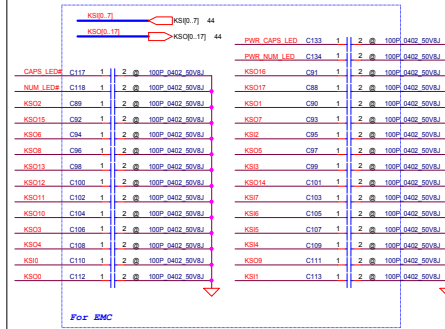
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Issued Date				2013/08/08				Deciphered Date		2013/08/05		Size	
Document Number				Custom				Date		Thursday, December 19, 2013		Sheet	
42				of				59		ACLU1 & ACLU2			



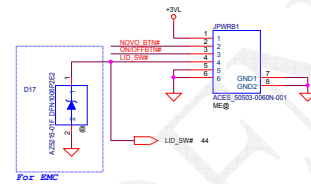
ON/OFF switch



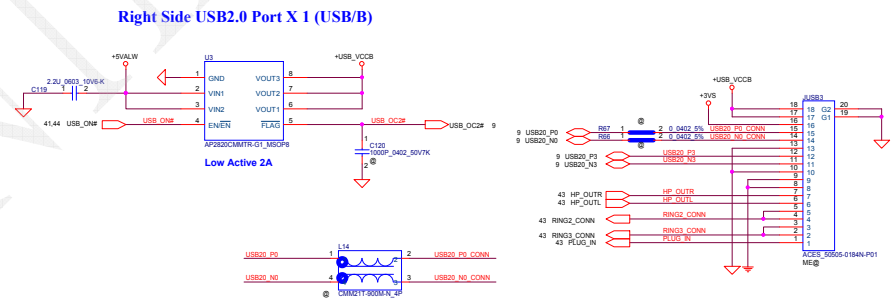
K/B Connector



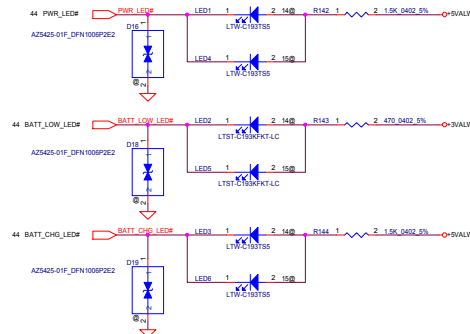
PWR/B Connector




USB I/O Connector

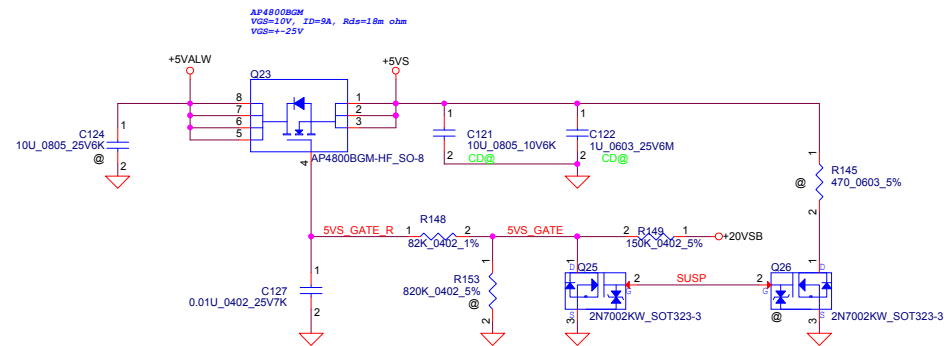


LED

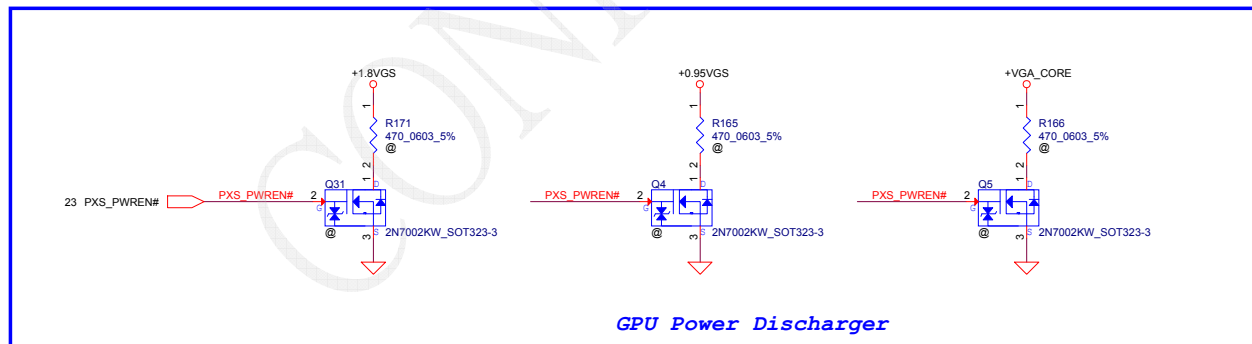
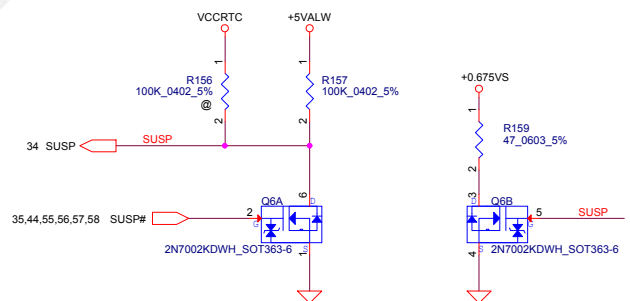
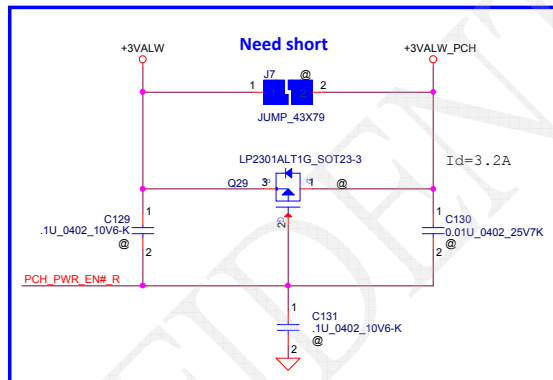
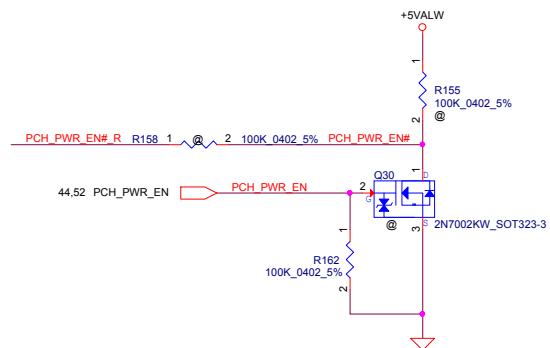
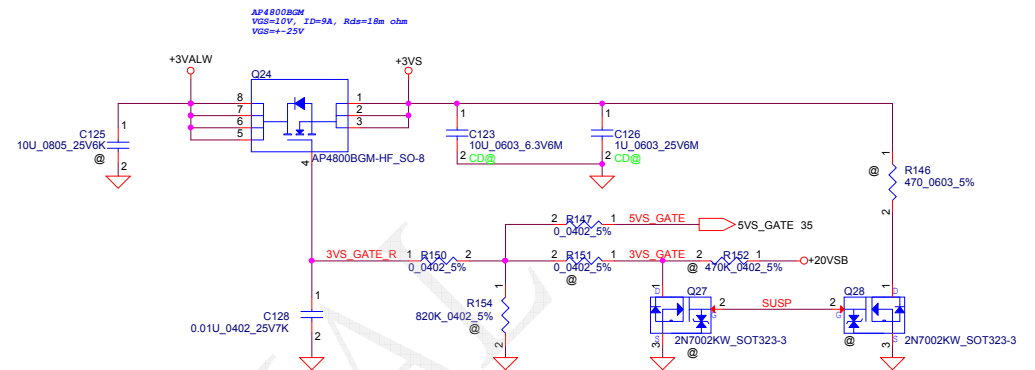


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Sheet Date: Thursday, December 18, 2013	Document Number ACUL1 ACUL02	Page 45 of 59		

+5VALW to +5VS

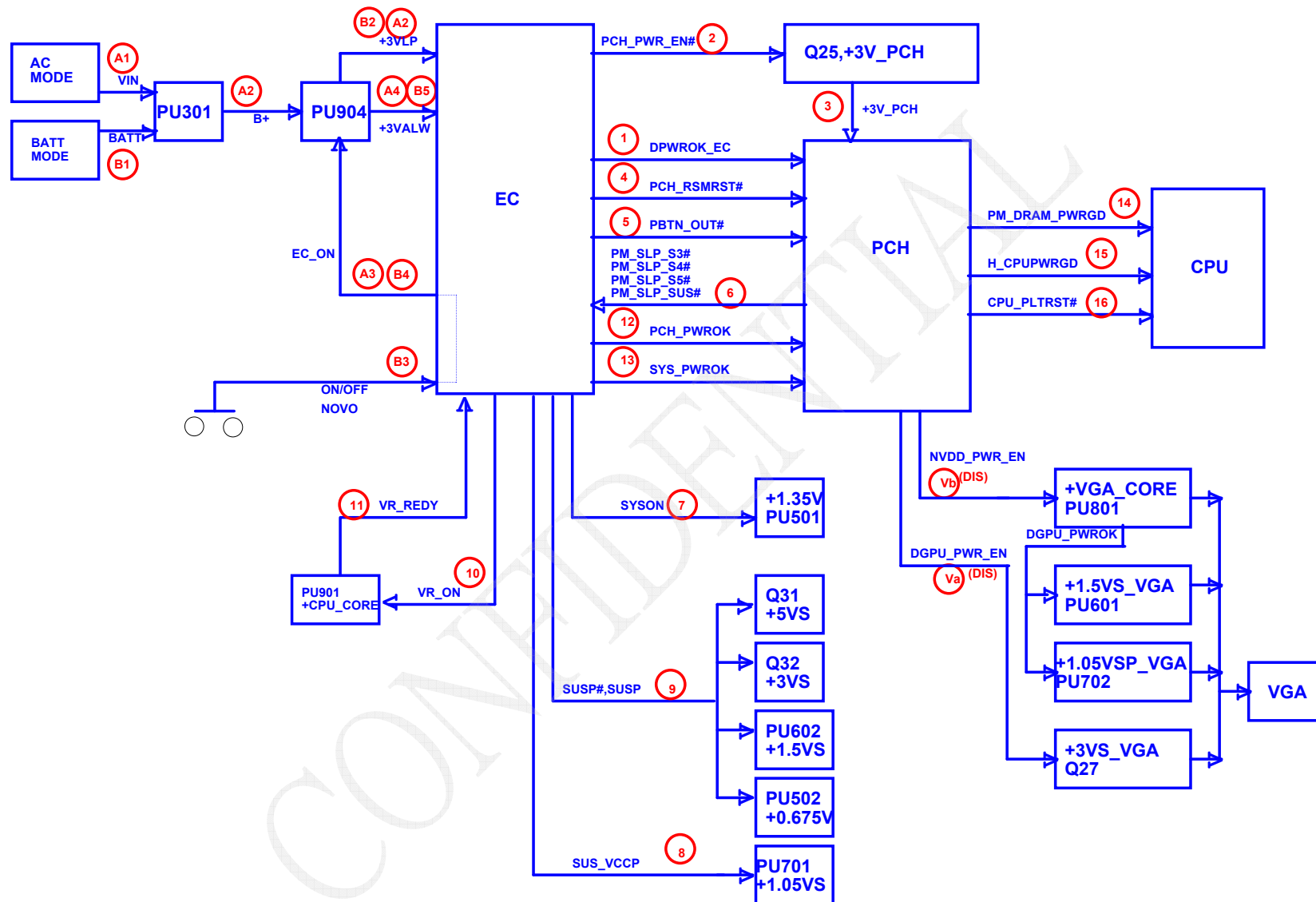


+3VALW to +3VS



GPU Power Discharger

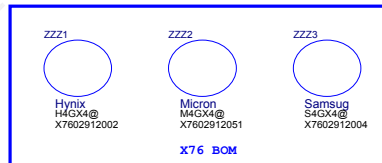
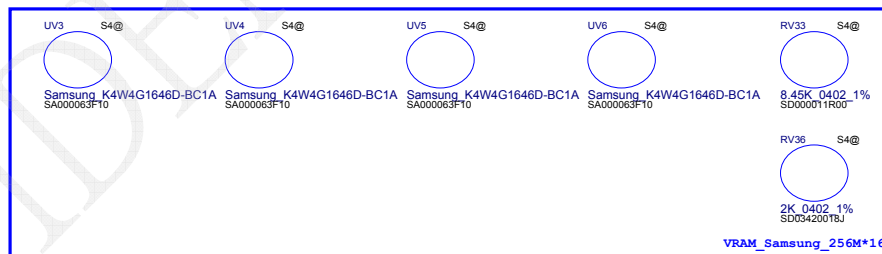
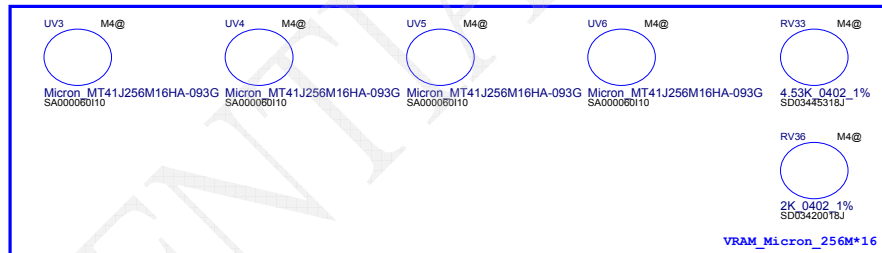
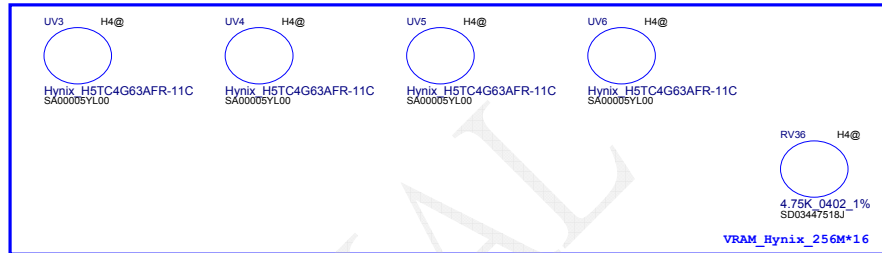
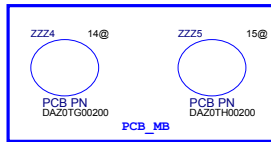
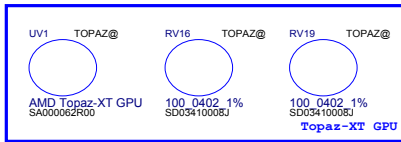
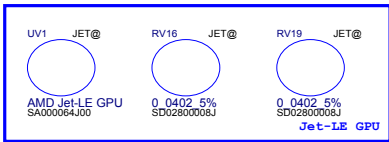
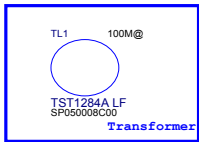
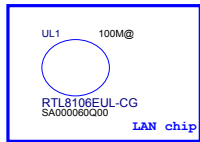
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Size		
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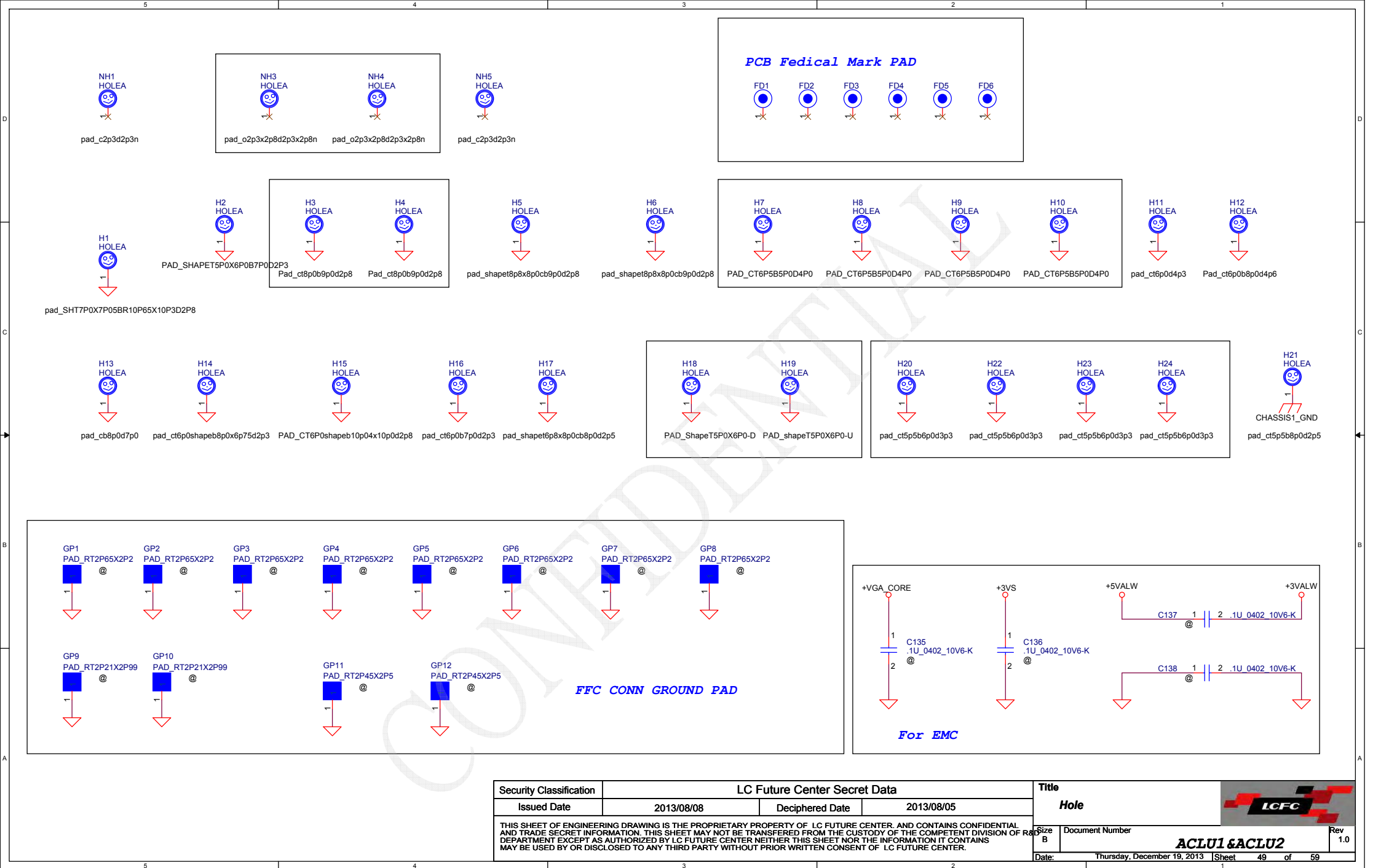
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Size	Document Number	ACL01 & ACL02	
Custom			
Date:	Thursday, December 19, 2013	Sheet	47 of 59

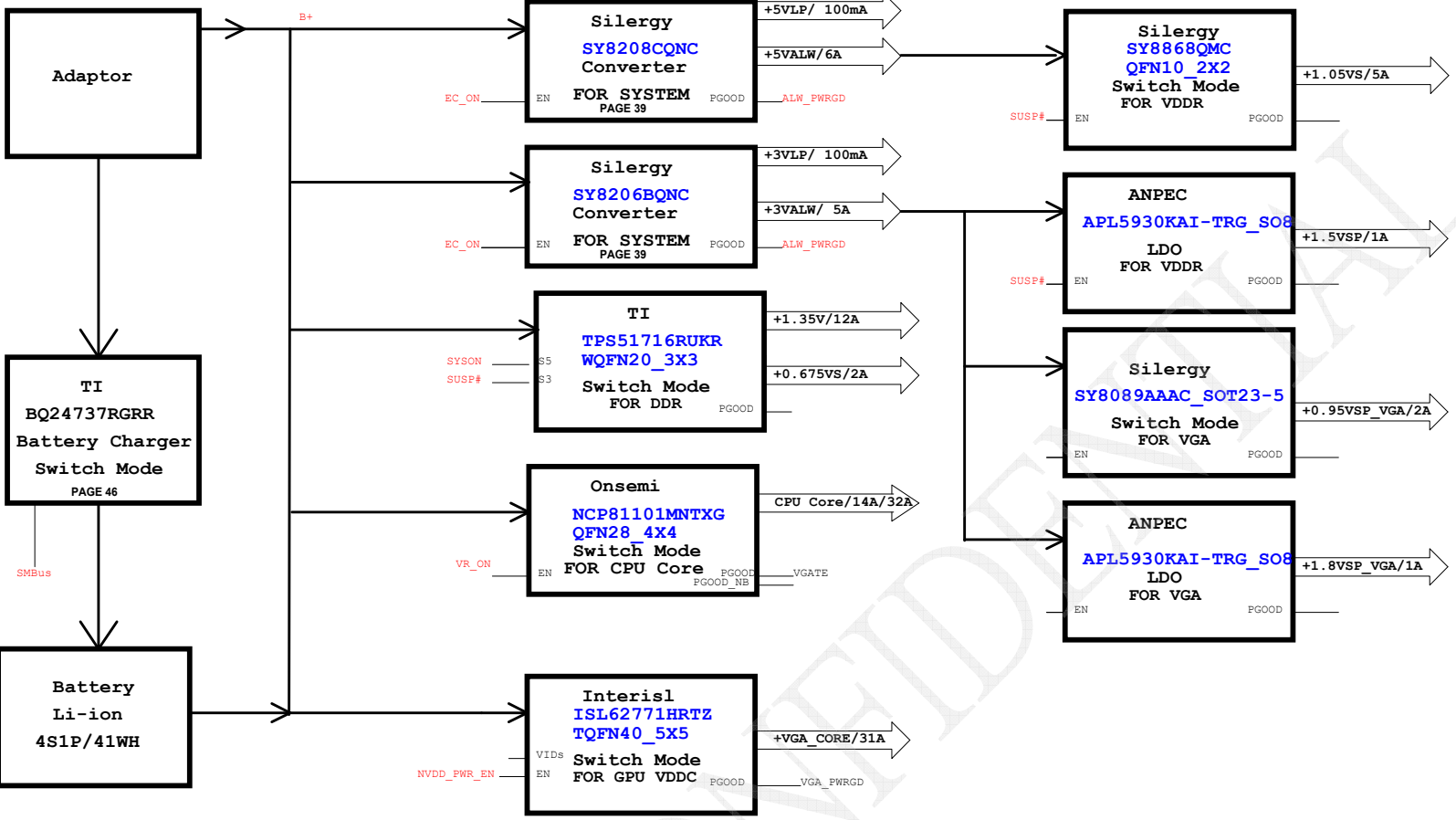




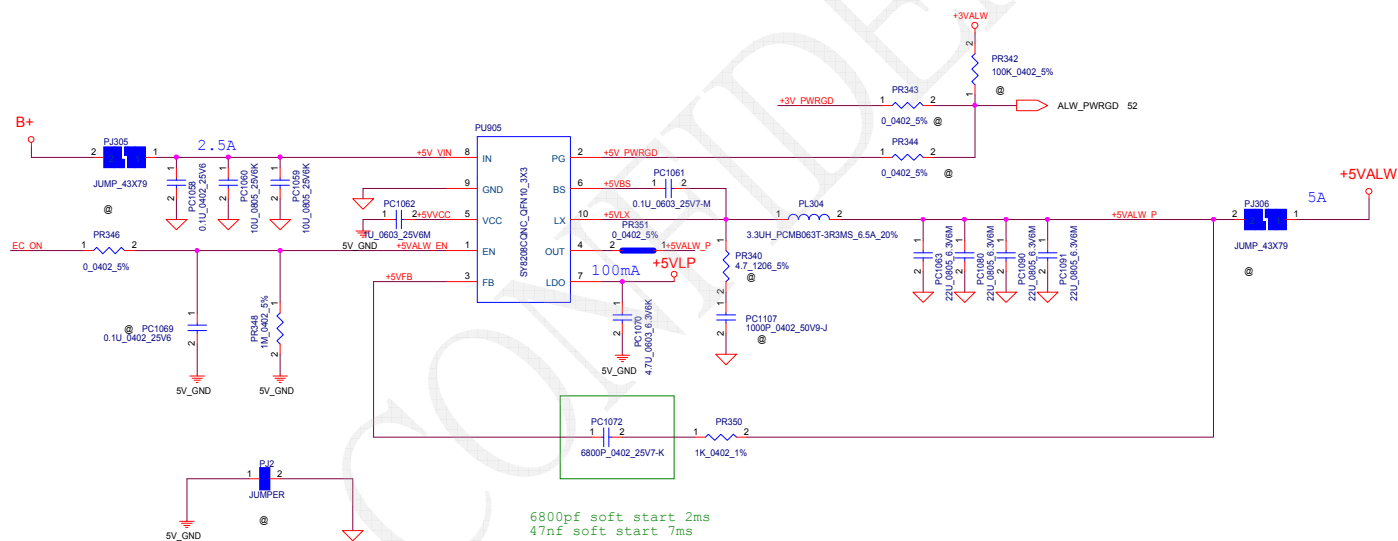
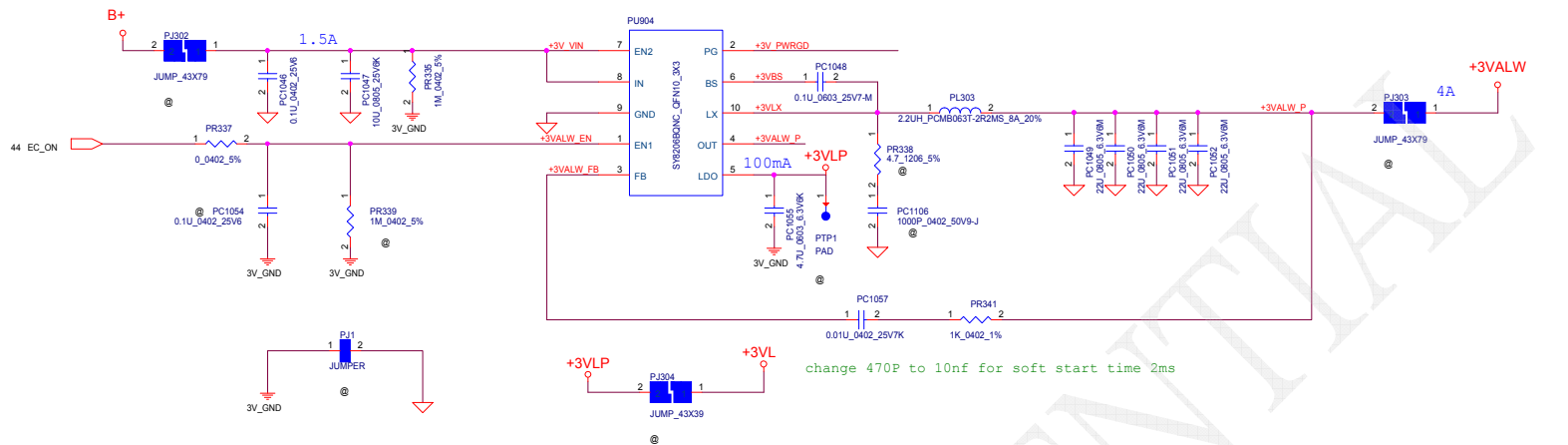
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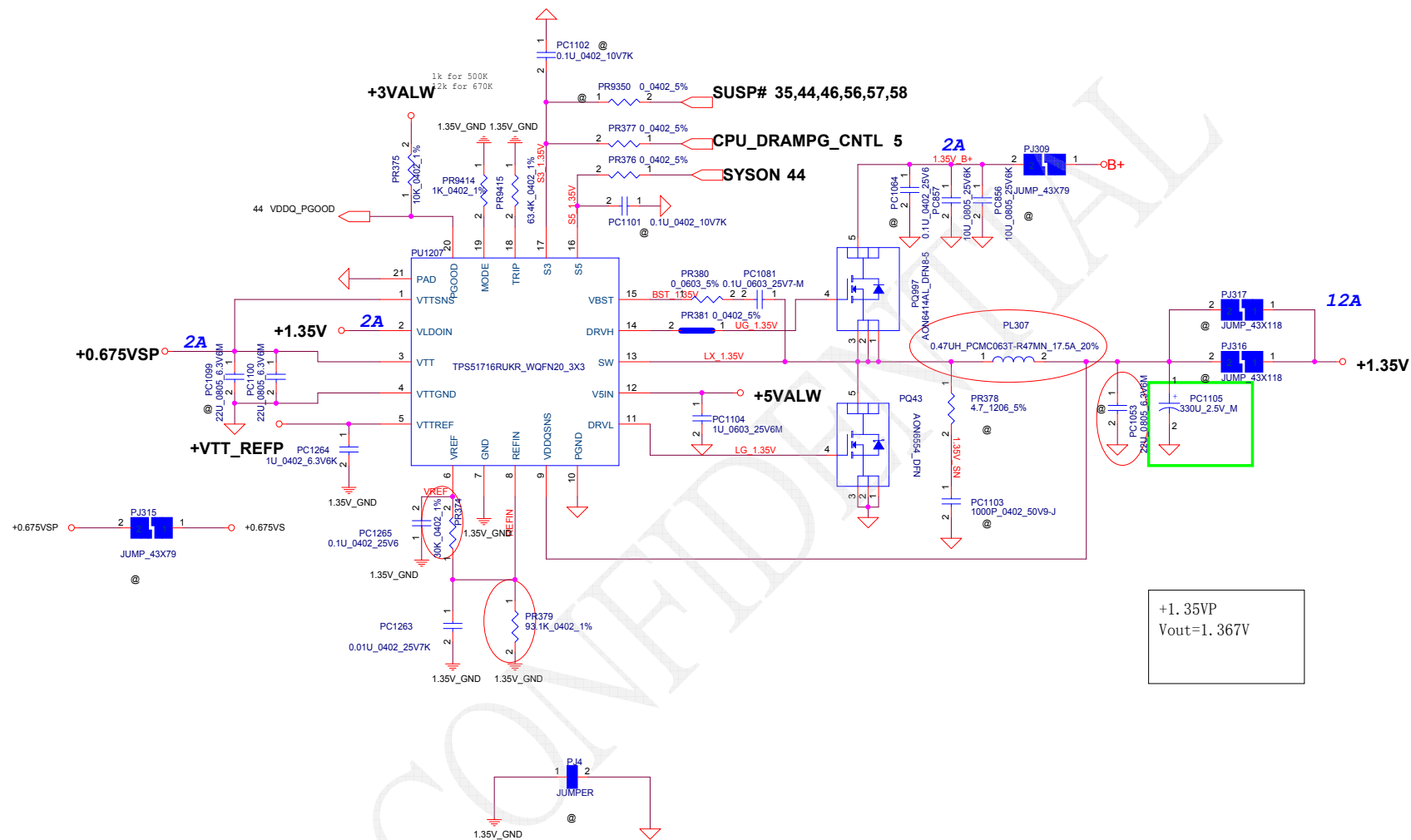
BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description	Stuff Resistor
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0	1	0	0	15" + Jet-LE sku	RC107,RC101,RC109,RC123
1	0	0	0	14" + Topaz-XT sku	RC100,RC108,RC109,RC123
1	1	0	0	15" + Topaz-XT sku	RC100,RC101,RC109,RC123

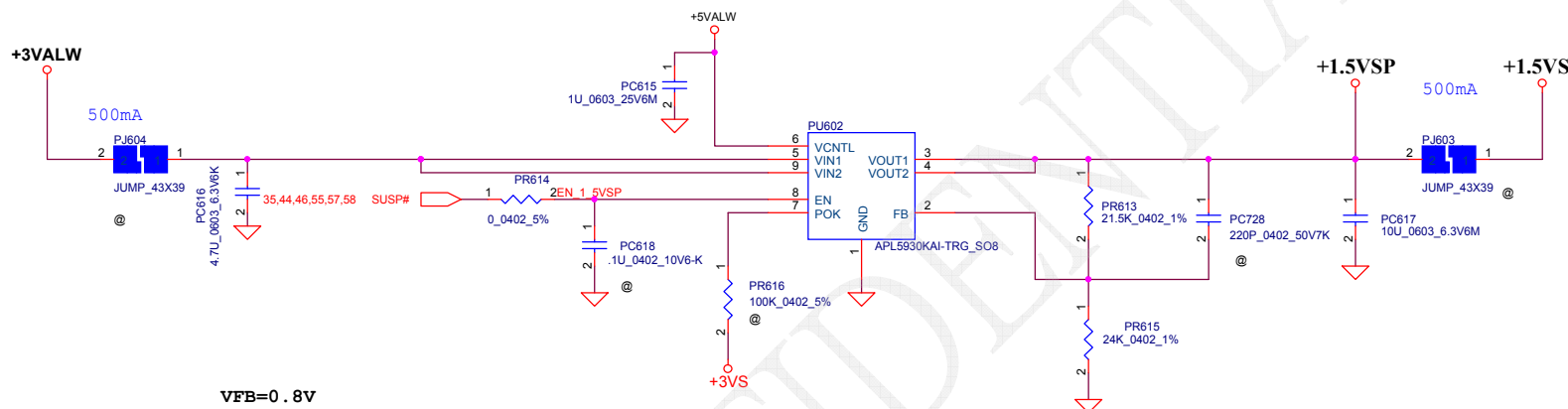




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				Date Thursday, December 15, 2013
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